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A Rail-To-Rail and Low Offset Novel Strongarm Comparator Circuit for Low Power Data Converter Architectures

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Abstract

With the rapid improvements in the design of advanced high performance communication receivers, hand-held electronic devices are in widespread usage for some time. These devices facilitate high speed and secured access to internet data. The demand for realizing a smart and better usage experience puts forth strict requirements on the design aspects of next-generation high speed low power complementary metal oxide semiconductor (CMOS) receiver design. One of the major modules in the implementation of high speed low power CMOS receiver device is the analog to digital converter (ADC) architecture. In the process of conversion from analog to digital signals, Quantization and sampling operations are vital and are realized using comparator circuits. The comparator design has a significant role in the design of data converter architecture. Several comparator architectures exist, but StrongARM topology is discussed and implemented in this work due to its negligible static power dissipation and rail to rail output voltages. The proposed novel comparator architecture is designed and simulated in 90nm CMOS process using Cadence Virtuoso tool and operated at supply voltage of VDD=1.5V, a clock frequency of 250MHz. Compared to the previous designs, the energy delay product was reduced by 8% which is an important observation to be observed for use in wireless sensor node applications.

Keywords: Comparator, Double-tail, Kick back noise, Low power, Single-tail, StrongARM.

Introduction

Technological innovations in the current century period have motivated professionals to make electronic gadgets smarter. These advancements are progressing at a brisk pace, facilitating faster changes and increase in computing power. Various technologies such as virtual reality, augmented reality, mobile internet, artificial intelligence, cloud computing, biometric devices, 3D printing machines, genomics, quantum computing, block-chain, industrial automation and robotics. In all these technologies, communications with nearby devices play a major role in its effective functioning. The fourth generation and fifth generation communications evolved to offer reliable and steadfast data transfer globally. At present the usage of high performance electronic gadgets enables high speed and safe access to the internet. The ever increasing demand of lower latency values, better connectivity, stable and high speed data transmission poses stringent requirements for next level high speed communication designs. The above high performance requirements are met by the inclusion of an efficient Analog to Digital Converter (ADC) architecture in the communication transceiver hardware. ADC architectures are essential and omnipresent in all receiver architectures.

ADC transforms a continuing time continuing amplitude voltages to distinct time distinct amplitude voltages and is random. It is a vital integrated circuit in a high performance analog radio frequency integrated circuit system and acts as interface in converting real-time signals to digital signals. It is vitally important that high speed ADC is very much essential for high speed transceiver architectures. The concerned parameter is sampling rate i.e. it specifies how fast the converter architecture is capable of sampling the continuous signal and converting it into discrete signal voltages. The influential modules in the accurate design and analysis of any ADC architectures are High-gain amplifier blocks and comparator circuits.

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Comparator circuit is otherwise called as Single-bit digital circuit. The selection and use of CMOS comparator circuit in the design of ADC architecture is crucial as it is mainly responsible in achieving the target specifications such as accuracy, speed, reduction of kickback noise and low power dissipation. Other specification include such as input referred noise, offset and hysteresis voltages. Several comparator architectures are available in the previous works such as Two-stage, Open-loop, Push-pull, comparator driving large capacitive loads, Singe-tail, Double-tail, Triple-tail latch, Switched capacitor comparator, StrongARM comparator, Regenerative comparators, Fully-differential two and three stage latch comparators, and high speed comparator circuits comprising of cascaded preamplifiers, latches and output driver circuits. Circuit designers often trade-off with different specifications and prefer double-tail comparators for use in high speed data converter circuits. In general a comparator circuit is implemented by a differential pair consisting of P-channel and N-channel metal oxide semiconductor transistors (MOS) followed by an active load stage, decision stage and an amplifying stage. For high speed circuits additional amplification stage may be added to the circuit. Figure 1, shows the different stages in a typical comparator circuit.

A comparator circuit compares two signal voltages (given input voltage with a standard reference voltage) and outputs a discrete value i.e. logic high or logic low. It can also be used to compare a signal whether it is above zero or below zero voltage. The input pre-amplifier circuit stage consists of a differential pair with active loads. This stage provides sufficient amplification before it is fed at the output stage.

Another important function of this stage is to reduce the inherent kick-back voltage generated by the decision stage. The decision module or latch module is the core section of the comparator circuit. Some amount of hysteresis is included in the circuit to reduce the small levels of noise occurring at the input side of the circuit. This stage determines which of the input signal voltage is larger and amplifies the difference of both the input voltages. The circuit should also be capable of distinguishing input signal voltages lying in the range between microvolts to millivolts. The gain of the circuit should be higher so as to provide positive feedback in the circuit. The final stage also known as post-amplification stage is necessary to avoid the loading effect of the next following stages. It generally includes an inverter circuit preceded by a self-biased input differential stage and the output voltage should not suffer from slew rate restrictions.

The original StrongARM latch configuration for a 0.512MB high-speed static RAM circuit at Toshiba corporation (1). It includes a low powered current controlled latch sense amplifier for memory and interface circuits and the simulation results demonstrate the access time (pico-seconds) is minimized. The StrongARM comparator circuit is a familiar and extensively used topology in data converter architectures and flip-flop circuits for various high speed and low power transceiver circuits (2). It is a unique and robust circuit with features such as high sensitivity, offers rail-to-rail output voltage, very high input impedance for time varying signals, low input referred offset voltage arising due to only one differential pair and virtually no static power dissipation (3).

The design of a pre-amplifier based dynamic bias latch type comparator under 0.065 micrometer technology and compares the design with a double-tail latch type comparator circuit is described in (4). The simulated results validate that the proposed work i.e. pre-amplifier based dynamic bias latch type comparator draws less power and a medium level reduction in input referred noise voltage than a double tail circuit architecture. A low powered double tail comparator architecture design with systematic expressions is presented in (5). Additional transistors in between the stages enhance the positive feedback of the circuit and thereby increase the speed of operation of the circuit. The simulation results in 180nm CMOS process technology exhibits a power consumption of 1.4mW, operated at a clock frequency of 2.5GHz with V_{DD}=1.2V. Two novel circuit schemes to reduce the kick back noise (i.e. voltage deviations in the circuit nodes are feedback to the input side to generate unstable voltages at the output node) were presented in (6). Simulation results confirm the minimization of kick back noise present in the comparator circuit. To compensate for offset voltages and lower noise, the design presented in (7) discusses modified strongArm latch circuit

parameters, whereby the noise bandwidth and input-referred offset voltage is reduced. An enhanced strongARM latch architecture based on forward body biasing method is mentioned in (8). This proposed method is simulated in 0.065 micrometer CMOS process and is based on the clock fine-tuning of the threshold voltage (V_T) of the cross-coupled NMOS transistors. A parallel path based strongARM latch comparator circuit implemented in 0.065 micrometer CMOS process in described in (9). The technique is implemented by inserting parallel paths to the output side of the circuit. Simulated results prove that the propagation delay decreases by 50% compared to the previous methods. The implementation of conventional and modified StrongARM Latch architectures is discussed in detail in (10). The presented work provides the importance of the StrongARM latch topology for various applications. A high speed double-tail comparator circuit with less variation levels in common mode voltages are presented in (11). The cascaded transistors reduce the kick-back noise also in this method under power supply voltage levels. The analysis of the effects of common mode voltage with respect to offset voltage, power consumption, noise and propagation delay in comparator architecture is presented in (12). The comparator architecture has been implemented in an energy efficient successive approximation register analog to digital converter architecture. A novel strongARM latch circuit design simulated in 0.065 micrometer CMOS process is described in (13). The proposed technique offers a latching speed of sixteen percentage compared to the other works as reported in the paper. The design and simulation of high speed dynamic bias comparator architecture for use in a second order sigma delta architecture is presented in (14). The aspect ratios of the input differential stage are modified to achieve the higher gains which resulted in the operating speed of the comparator circuit. The design and analysis (transient and noise) of a pseudo-differential dynamic comparator is carried out in 90nm CMOS process technology (15). Two calibration methods such as load capacitance and bypass current are discussed along with its process, voltage and temperature (PVT) variations. The strongARM latch design architecture using auxiliary pair reported in (16) discusses the design equations to optimize the various parameters such as offset voltage, input-referred noise voltage and decision time in detail. The rest of the paper is organized as follows: Section-2 discusses about the proposed modified strongARM comparator architecture along with its working details, while Section-3 provides the simulated results and its discussion. Lastly Section-4 presents the conclusions of the proposed work.

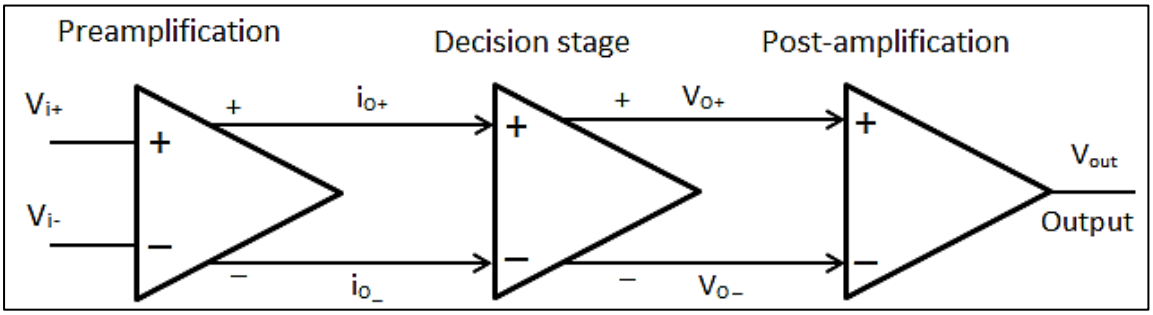

Figure 1: Inner blocks of a Comparator circuit

Materials and Methods

The proposed modified StrongARM comparator circuit shown in Figure 2 operates in different phases namely reset, amplification and regeneration. The circuit consists of MOS switches M_{S1}, M_{S2}, M_{S3} and M_{S4}, a differential pair with a clock source (V_{CK}) and triple cross-coupled differential pairs (M_1 & M_2), (M_3 & M_4) and (M_5 & M_6). The tail transistor is driven with a clock source. The differential output voltage is taken at the drain nodes of M_5, M_6, M_7 and M_8. Correspondingly, the voltage at these nodes is designated as V_A and V_B. The main feature of this proposed StrongARM configuration is that it delivers rail-to-rail output voltages at nodes A and B.

The circuit responds to difference in the input voltages (V_{i1}-V_{i2}). In the first phase when the clock voltage is low i.e. V_{CK}=low, then the transistors M_1 and M_2 are off and accordingly the internal capacitances at nodes A, B, X and Y are precharged to the supply voltage V_{DD} through the MOS switches M_{S1}, M_{S2}, M_{S3} and M_{S4}.The next stage is the amplification phase, which gets initiated, when the clock voltage is high i.e. V_{CK}=high. With these connections, the MOS switches M_{S1}, M_{S2}, M_{S3} and M_{S4} are off and the charged voltage gets discharged through M_7, while M_1 and M_2 are conducting. Transistors M_1 and M_2 are biased by a constant common mode voltage (V_{CM}). When there is a small difference in differential currents applied at M_1 and M_2 due to minute differences in (V_{i1}-V_{i2}), then the capacitances at the nodes X and Y are discharged at marginally different discharging rates.

When voltages at X and Y drop to (V_{DD}-V_{tn}), transistors M_5 and M_6 turn ON. In this phase, the voltage |V_X-V_Y| increases and certainly beyond (V_{i1}-V_{i2}). Hence in this stage, voltage amplification is achieved. Assuming $g_{m\,1,2}$ as the transconductance of the input transistors M_1 and M_2, the voltage difference is written as

$$|V_X - V_Y| = \left(\frac{g_{m\,1,2}\,(v_{i1}-v_{i2})}{C_{X,Y}}\right) * t \quad [1]$$

The voltage gain in this phase is given by

$$A_V = \frac{g_{m\,1,2,3,4} * V_{tn}}{I_m} \quad [2]$$

When the available voltage at nodes A or B reduces to the difference between the power supply voltage and threshold voltage of the p-type MOS transistor, due to this transistors M_7 or M_8 will be switched on to conduct, while the transistors M_5, M_6, M_3, M_4 remain in off state. Due to this operation, the voltage at nodes A or B reach either V_{DD} or logic low or vice-versa. The offset voltage is minimized by reducing the precharge operation of the MOS switches M_{S1}, M_{S2}, M_{S3} and M_{S4}.

Results and Discussions

The design and simulation of the proposed strongARM comparator circuit is carried out in 90nm CMOS process and the simulated transient analysis waveforms obtained at node 'A', Node 'B' and clock signal are displayed in Figure 3. The waveform consists of reset phase, amplification phase and regeneration phase. When the input differential voltage becomes more than or equal to 0.005V, then the comparator output produces a rail-to-rail swing voltage at the output side. The inherent clock feed through problem becomes negligible in both reset and amplification phases. In this proposed design, the amplification phase and regeneration phases operate slower than the reset phase time-periods.

The simulated graphs related to the propagation delay (ps) versus differential input voltage are presented in Figure 4. The results illustrate that the proposed comparator circuit operates at lesser delay and correspondingly at higher speeds. The graphs illustrate that as the difference voltage (V_{i1}-V_{i2}) increases; there is a matching increase in operating speeds.

The simulated graphs related to the energy consumption (fJ) versus differential input voltage are displayed in Figure 5. The results illustrate that the proposed comparator circuit operates at reduced power levels. The graphs confirm that as the difference voltage (V_{i1}-V_{i2}) increases, there is a corresponding decrease in energy consumption levels. Table 1, presents the obtained values of propagation delay (ps) versus differential input voltage (v), while Table 2, shows the energy consumption versus differential input voltage (v).

Figure 6, presents the simulated common mode voltage versus energy delay product. Figure 7, displays the simulated input referred noise voltage versus overdrive voltage which indicates as the difference between the gate to source voltage and threshold voltage increases, correspondingly the input referred noise voltage varies linearly within acceptable limits.

A large value of g_m/I_D is very much essential for enhancing the noise performance of the proposed strongARM comparator circuit. With increasing values of overdrive voltages, g_m/I_D decreases, thereby reducing the input referred noise voltage. The simulated graph results between g_m/I_D and overdrive voltage is presented in Figure 8. The simulated offset voltage curve variation with respect to varying common mode voltages is presented in Figure 9.

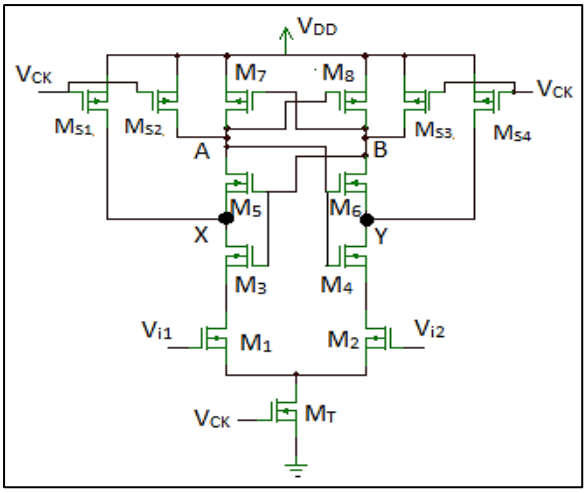

Figure 2: Proposed StrongARM comparator circuit

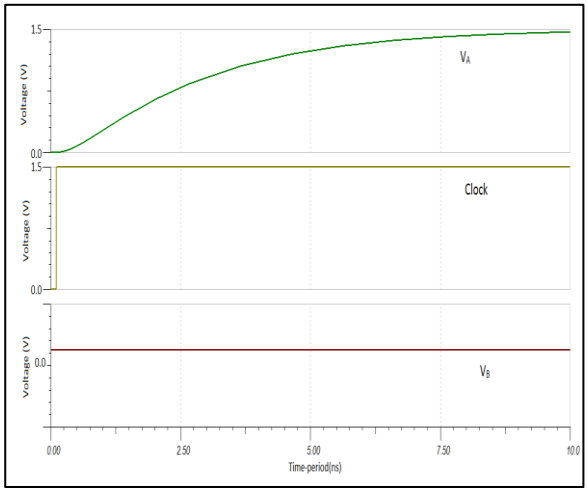

Figure 3: Simulated transient analysis wave forms

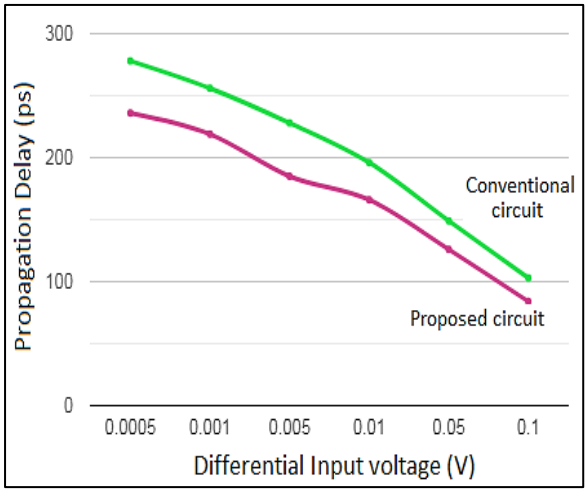

Figure 4: Simulated propagation delay versus differential input voltage

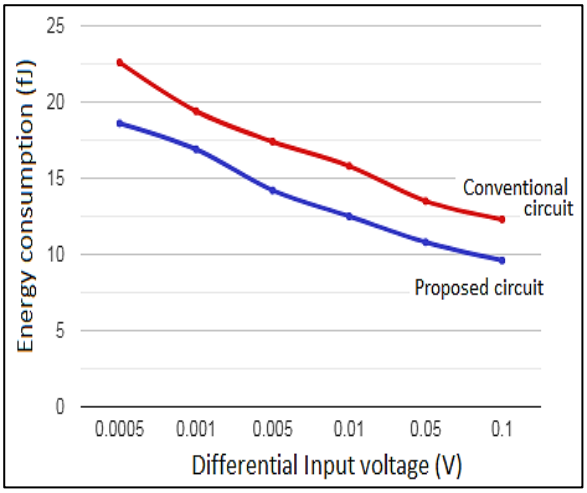

Figure 5: Simulated energy consumption versus differential input voltage

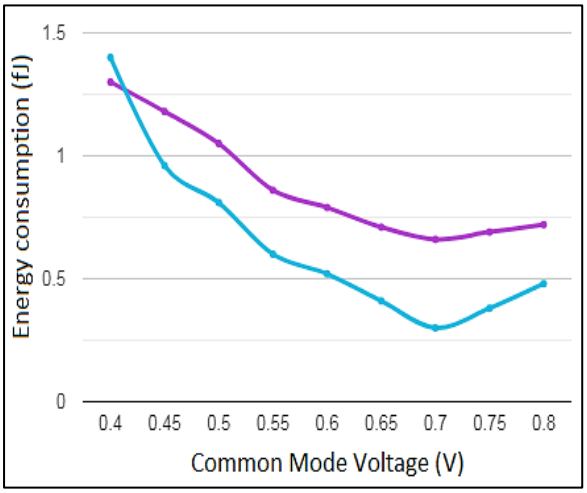

Figure 6: Simulated energy consumption versus common mode voltage

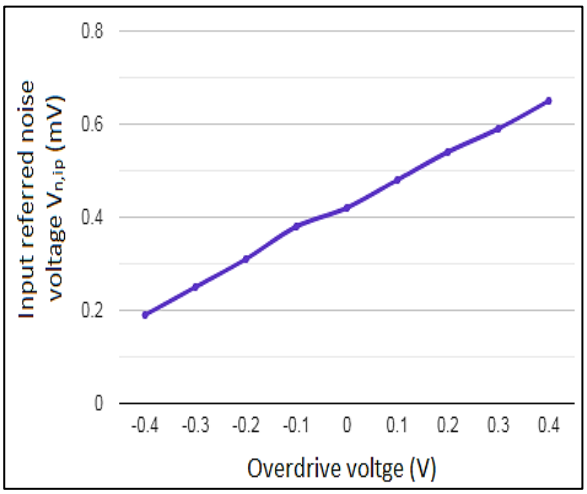

Figure 7: Simulated input referred noise voltage versus overdrive voltage

Table 1: Simulated values of Propagation delay

Differential Input voltage (V)	Propagation Delay (ps)	
	Conventional	**Proposed**
0.0005	278	236
0.001	256	219
0.005	228	185
0.01	196	166
0.05	149	126
0.1	103	84

Table 2: Simulated values of Energy consumption

Differential Input voltage (V)	Energy consumption (fJ)	
	Conventional	**Proposed**
0.0005	22.6	18.6
0.001	19.4	16.9
0.005	17.4	14.2
0.01	15.8	12.5
0.05	13.5	10.8
0.1	12.3	9.6

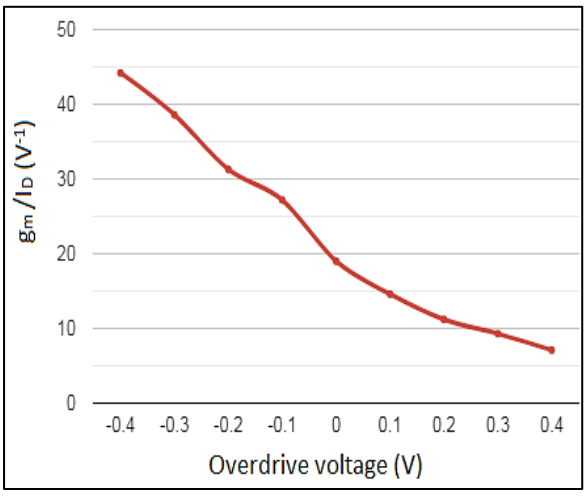

Figure 8: Simulated $\left({g_m}/{I_D}\right)$ and overdrive voltage

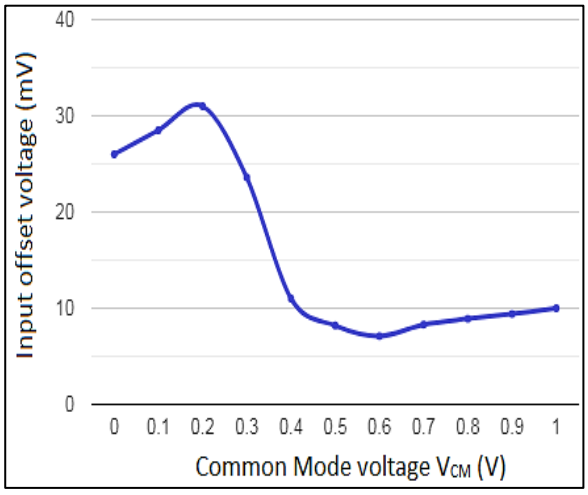

Figure 9: Simulated input offset voltage versus common mode voltage

Conclusions

In this proposed paper a modified novel strongARM latch circuit is designed and implemented for low power data converter architectures. The preamplification and primary decision operations are carried by a single stage strongARM latch circuit. The architecture shown here provides a very low overhead result to reduce the energy consumption. The performance of the comparator can be enhanced for a given common-mode voltage by varying the aspect ratios of the input differential stage and the tail transistor. The proposed comparator circuit is designed and simulated in 90nm CMOS process using Cadence Virtuoso tool and operated at supply voltage of VDD=1.5V, a clock frequency of 250MHz. Simulation results demonstrate that the propagation delay is reduced by approximately 7%, energy consumption slightly decreases by 4% and overall energy delay product decreases by 8% when compared to the previous designs. Consequently, the applications that demand low power operation, such as internet of things (IoT) nodes or monitoring of wireless sensor nodes, the proposed strongARM latch comparator circuit would be an interesting choice for such remote applications.

Abbreviations

Nil

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Nil

Authorship contribution

K. Lokesh Krishna: Conceptualization, Methodology, Software, Data curation, Writing – original draft, D. Srinivasulu Reddy: Visualization, Investigation, Supervision, Software, T. Chandra Sekhar Rao: Validation, Writing – review & editing.

Conflict of interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Ethics approval

The research does not involve human participants.

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