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Implementation of Shunt Active Power Filter in Three Phase Inverter for Fault Detection and Mitigation of Harmonics

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Abstract

The power quality domain in power system networks has received more attention recently because of the increase in sensitive equipment, non-linear load disturbances, and the utilization of Renewable Energy Sources (RES). In case of distributed generation, which could occur from consumers to utilities, power quality quantifies the suitability of electric power supplied from the utilities to the commercial, industrial, and residential users. A minimum of half of the total disruptions to power quality are related to voltage quality. This research concentrated an amplitude-frequency estimation based methods, Power quality Disturbance Classification and Filtering techniques for harmonic mitigation. The enhancement of power quality in a three-phase nonlinear load power system is the subject of this research. Shunt Active Power Filter (SAPF) is used in real-time applications for fault detection and harmonic suppression. The suggested work uses a digital signal processor (DSP) (28335) and a shunt active power filter (SAPF) to achieve power quality disturbance detection and harmonic reduction on hardware system. In addition to applying shunt compensation devices for harmonic detection, the designed hardware model is tested for power quality disturbance categorization of voltage sag, harmonics, and interruption and Total Harmonic Distortion (THD) is 4.3% in this case. The overall implementation of the hardware using -Fuzzy algorithm is found to be satisfactory.

Keywords: Digital Signal Processor (28335), Fuzzy Logic Controller, Sensor, Shunt Active Power Filter, Three Phase Inverter.

Introduction

The growing use of non-linear loads and the frequency of electrical system breakdowns have resulted in a decrease in the quality of energy supplied to consumers. Harmonics, transients, flicker, voltage sag, and voltage swell are among the often occurring power quality disruptions. Detecting and identifying the source of the power quality issue is crucial to improving the quality of the supplied electric power. As a result, equipment for monitoring power quality has significantly advanced. Because of this, an automatic recognition method for classifying the disturbance waveform must be developed (1). Harmonics in the power system are mostly caused by such non-linear devices, inspite of the fact that power electronics devices have benefited the electrical and electronics industries. A periodic wave's harmonic component is sinusoidal, utilizing a sine wave multiple fundamental wavelengths as a frequency. The quality of the power supply will be lowered by these power harmonics, also known as electrical pollution. Moreover, they disrupt neighboring communication networks, disrupt other users, and have low power factor and system efficiency (2).

The significant loss that results from anomalies such disruptions or variations in frequency, current, and voltage during the delivery of electricity creates a severe disadvantage in such a scenario. Equipment efficiency is decreased as a result of electrical and electronic components malfunctioning (3). A lot of attention has been paid in recent decades to the topic of advancements in technical tools for power difficulties because of new and inventive trends and technology in this field. Unbalanced loads are the result of frequency mistakes brought on by power quality issues. As a result, Power Quality (PQ) events must uphold power supply source criteria. It needs to be kept an eye on and managed (4, 5). Finding and implementing high-performance solutions to enhance power quality, as well as innovative

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mechanism strategies that perform improved in current schemes, are therefore highly relevant. The traditional low-cost passive filters that are used to balance reactive power and harmonics have the drawbacks of being large and inflexible when system parameters change. Furthermore, they have poor harmonic filtering performance (6, 7).

The most cutting-edge method for achieving the best reactive power, load imbalance, and harmonic compensation is generally acknowledged to be the employment of active power filters (APFs), which are devices based on power electronic converters. It is the most often used of these to enhance electrical power systems' power quality (8). It injects a suitable compensating current in the point of common coupling (PCC) created in accordance with the intended compensation strategy after being linked in similar with the nonlinear load. The application of SAPF has drawn a lot of interest from international laws pertaining to quality of electricity measurement and harmonic control (9-11). Numerous accomplishments in various areas pertaining to the creation of filtering systems have been verified, and there is now demonstrated interest in this field. In addition to the conventional SAPF scheme, Alternative electric circuit arrangements for three-phase SAPF have been suggested (12-14).

For applications requiring substantial power, precise compensation can be achieved by utilizing the SAPF architecture using a kind of parallel level DC-AC Converter linked to the same AC line and sharing a single DC-link capacitor. Additionally, compared to the traditional setup, harmonic distortion is reduced and it is possible to raise SAPF output voltage values increased (15, 16). To optimize the current waveform and reduce the voltage stress in the components of the inverter, multilevel schemes utilized in a significant voltage and substantial power instead of the conventional two-level design. Three inverter levels are the most allowed in most SAPF systems to lessen the impact of voltage imbalance in the DC-link capacitors (17).

Three-level inverter topologies that are frequently utilized for SAPFs are Cascaded H-bridge (CHB), Flying Capacitor (FC), and Neutral Diode Clamped (NPC) (18). The three-level NPC topology is the most popular among them because it uses the fewest DC capacitors, which results in a smaller physical size and less issues with the DC-link voltage imbalance (19). New power semiconductor devices, such as SiC and GaN transistors, which switch at very high frequencies with lower switching losses than the widely used IGBTs (Insulated-Gate Bipolar Transistors), can now be used in the Electric circuit configuration of the SAPF to advancements in power electronics technology in recent years (20).

As a limitation of previous research, a lower power factor, and increased system energy costs, harmonic power quality disturbances increase the amount of power needed by the system. Electrical harmonics in a system are filtered away using a harmonic filtering procedure. The shunt active power filter is a self-regulating direct current bus that combines a topological structure with static compensating devices. In power transmitting systems, this is utilized for reactive power adjustment. This shunt active filter uses a number of design elements, including ripple filters, power circuits, control circuits, and control techniques. By injecting an equal-but-opposite harmonic compensatory current, this filter assists in mitigating the harmonics of load current. During that moment, this filter functions as a source of current, injecting harmonic components that would typically need to be generated with the assistance of a load, but with a 180-degree phase shift.

Power quality monitoring is a standard procedure for utilities due to the increased demands on oversight and management in contemporary power systems. Electric utilities routinely monitor power provided at client sites to enhance power quality. To classify and examine power quality disruptions, power quality monitoring is required. Typically, Voltage and current are continually measured over a long period of time using power monitoring recorders to gather data. Power monitoring devices continuously record disturbance waveforms, generating gigabytes of data annually. The huge volume of data creates a number of real-world issues with data transmission and storage from local monitors to central processing systems.

Based on the detailed survey of the literature in the proposed area, it has been found that monitoring and classifying the different power quality disturbances, harmonic suppression using the installation of a shunt active power filter with

Fuzzy Logic Controller (FLC) have become more important research area in power system.

As discussed in literature survey, several techniques have been proposed for monitoring and classification of PQ disturbances and different control strategies used for harmonic mitigation. The monitoring and classification of PQ disturbances is the most fundamental requirement in the areas of various signal processing techniques because it is the basic requirement for the transformation and Decomposition based signal processing techniques, amplitude-frequency estimation-based methods and Categorizing power quality issues by the use of neural network techniques. There is a gap in the investigation of suitable methods for monitoring the power quality disturbances by Neuro Fuzzy System (NFS) System, Mitigation of Harmonics using active filters by FLC.

Methodology

Several techniques have been proposed for monitoring and various control techniques for harmonic abatement and the categorization of power quality disruptions. The detecting and categorizing PQ issues is the most fundamental requirement in the areas of various signal processing techniques because it is the basic requirement for the transformation and decomposition-based signal processing techniques, amplitude-frequency estimation-based methods and identifying power quality issues using Neural Network Approaches. Further, mitigation of harmonics using shunt active filter by harmonic extraction method to improve the power quality in the power system is also discussed. Recently, creations of an effective power quality detection system and a harmonic suppression active filter design have been used to classify the PQ disturbances and also to estimate and mitigate the harmonic presents in the power system.

The suitable methods for monitoring the power quality disturbances by Neuro Fuzzy System (NFS) Classifier and Mitigation of Harmonics using active filters by Fuzzy Logic Controller (FLC).This proposed method focused a Neural Network Approaches for Power quality Disturbance detection and classification and Filtering techniques for harmonic mitigation.

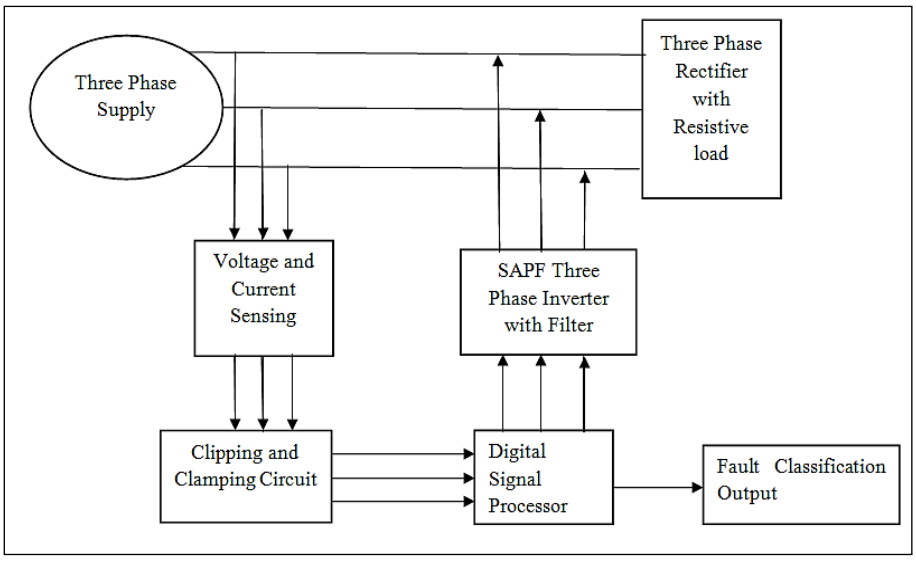

Figure 1: Schematic Diagram of Proposed System

Proposed Implementation

The classification problem receives the voltage and the current waveform from the power system and classifies the type of fault. Hilbert Huang Transform is applied on the current and the voltage waveform and trained on the Neuro Fuzzy System (NFS). The trained model of the NFS is embedded on the DSP 28335 with all the tuned hyper parameters. The trained model will classify the type of fault from the voltage and the current sensed. The SAPF comprises of, three-phase inverter, DC link capacitor and a filter is shown in Figure 1. The two-bus system which has the three-phase power supply with the nonlinear load linked to it at the second bus is compensated by the SAPF inverter.

The Schematic diagram of the overall hardware implementation is shown in the Figure 1. It shows

the fault classification output which is obtained from the NFS trained model on the DSP controller. PI controllers use mathematical models with proportional and integral terms to adjust control output based on error, suitable for linear systems with predictable behavior. FLCs, on the other hand, use human-like reasoning and linguistic terms like "high" or "low" to handle uncertainty and imprecision, making better suited for complex, nonlinear systems where traditional PI tuning is difficult.

The three-phase supply is used from the mains with a three-phase transformer to bring the voltage range to around 140V. After connecting the three-phase rectifier to the three-phase supply, the nonlinear load is introduced. Resistive load is connected in parallel to the rectifier output. The disturbed current due to the nonlinear load introduces harmonics. This harmonic compensation is carried out using the three-phase inverter using the DSP28335 controller. The voltage and current sensed from the source side is clipped to provide the positive voltage and the clamped to bring the voltage within 3V range that is compatible to the DSP controller.

The input filter is chosen as inductor L_f= 3mH, C_f =2μF. Table 1 depicts the specifications for the SAPF topology.

Table 1: Parameters Used in the Proposed Two-Stage Converter

Component	Parameters	Simulation values	Hardware values
Grid side converter	Power	100kW	400 W
	Frequency	50 Hz	50 Hz
	Inverter output voltage	440 V	140V(peak)
	DC link voltage	880 V	112V
	Inductive filter	2 mH	60mH
Grid	Voltage	440 V	0-270V autotransformer
	current	20A	10A
	frequency	50Hz	50Hz

System with Conventional PI Controller

The DC link voltage $V_{dc,}$ measured is obtained as the result of the composite controller in the inverter. The measured DC link voltage is compared with the reference DC link voltage $V_{dc,\ ref}$ and the error in voltage is sent to Proportional Integral (PI) controller for getting reference d axis component for the hybrid controller at the grid side converter. Figure 2 shows the PI controlled DC-link voltage regulator used in the grid side converter. The DC link voltage is taken as 60% to 70% of grid voltage approximately.

System with Fuzzy Controller

Fuzzy controller is best suited to control DC link voltage of the inverter. It will increase the dynamic performance of the grid-connected system. The Schematic diagram of voltage regulator using Fuzzy-PI is displayed in Figure 3.

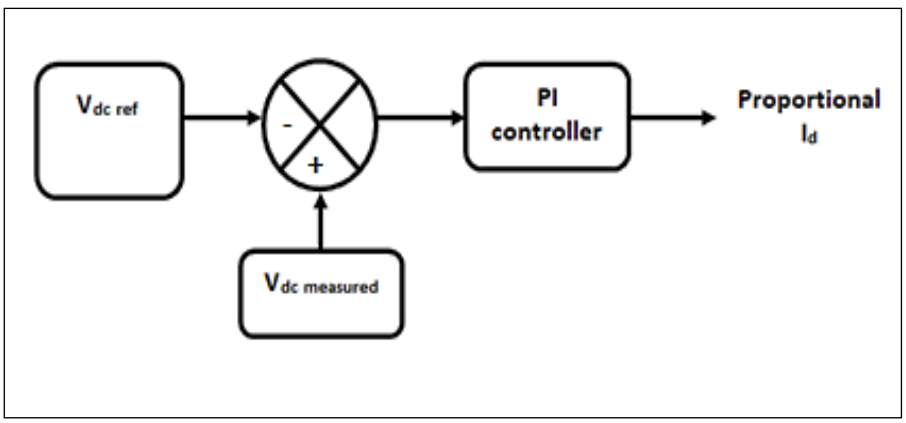

Figure 2: Block Diagram of PI Controlled DC Link Voltage Regulator

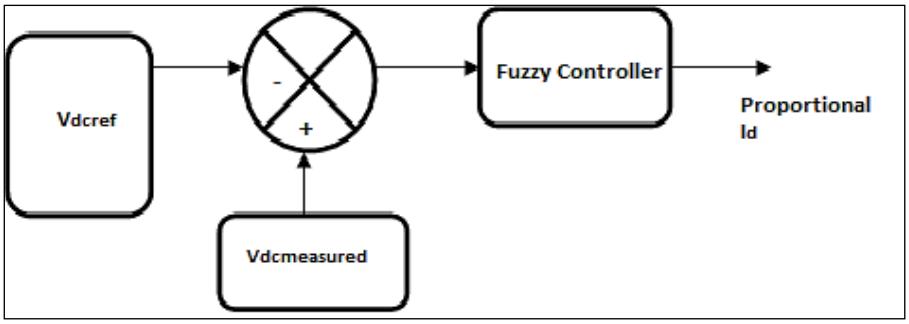

Figure 3: Schematic Diagram of Fuzzy Controlled DC Link Voltage Regulator

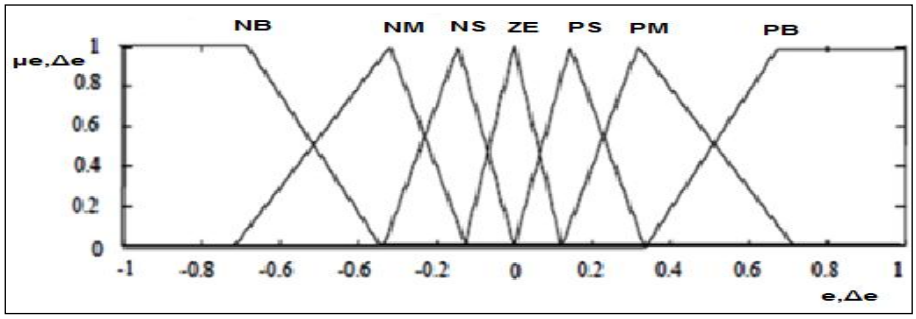

Figure 4: Output Normalized Membership Function I_{max}

Although FLC is claimed to be utilized, the rules, tuning process, and membership functions are not fully described. It would be beneficial to have a Table 2 or subheading for FLC design. Output Normalized membership function I_{max} is shown in Figure 4.

Fuzzification: The process of changing a numerical variable (a real number) into a linguistic variable (a fuzzy number) is known as "fuzzification".

Database: The membership function definition that the fuzzifier and de-fuzzifier require is stored in the database.

Rule Base: This rule base table's components are derived from the idea that high errors in the transient state necessitate coarse control, which calls for coarse input/output variables. Small mistakes in the steady state necessitate precision control, which calls for fine input/output variables. The FLC rule basis is listed in the Table 2.

De-Fuzzification: The FLC rules produce the necessary output in a fuzzy number, a linguistic variable, based on real-world needs; the fuzzy number must be converted to a real number, a crisp output.

Neuro-Fuzzy-based Shunt Active Power Filters (SAPFs) offer improvements over conventional SAPFs, particularly in handling complex scenarios and achieving higher performance. While conventional SAPFs rely on fixed algorithms, Neuro-Fuzzy integrates fuzzy logic with neural networks, allowing for adaptive and dynamic control based on system conditions. This results in better adaptability and robustness under varying voltage, load, and harmonic conditions. Neuro-Fuzzy-based SAPFs offer a significant advantage over conventional methods by enabling adaptive and robust control, leading to improved power quality performance. However, this comes with a higher complexity in implementation and potentially higher computational cost. THD value of FLC based SAPF under balanced condition is less than three phase power system with nonlinear load under unbalanced condition.

Table 2: Rules for Fuzzy System

Δe \ e	NB	NM	NS	EZ	PS	PM	PB
NB	NB	NB	NB	NB	NM	NS	EZ
NM	NB	NB	NB	NM	NS	EZ	PS
NS	NB	NB	NM	NS	EZ	PS	PM
EZ	NB	NM	NS	EZ	PS	PM	PB
PS	NM	NS	EZ	PS	PM	PB	PB

PM	NS	EZ	PS	PM	PL	PB	PB
PB	NB	NM	NS	EZ	PS	PM	PB

Experimental Validation of Proposed SAPF Converter

The experimental validation of the parallel inverter is observed in the simulation, carried out using MATLAB is validated using a scaled down implementation of the power. Considering the size and cost of the equipment the scaling down of the rating is inherited in the experimental implementation. Both voltage and the power regulation are targeted while the validation is experimented. The three-phase inverter used would use the scaled down voltage from 415V rms to 80V peak voltage since the implementation side is desired to have 80V with parallel inverter maintaining that voltage and synchronization. Hardware Specifications: MOSFET ---IRFP460-500V, 20A, Driver IC-IR2101, CD4050 Buffer IC, Inverter 1: 1.5 kVA, Inverter 2: 0.5 kVA.

System Description

The Experimental setup-schematic of the system which is shown in Figure 5 of the two-stage converter for the SAPF is emulated using the converter Setup comprising the three phase three level inverter with the Metal Oxide Semiconductor Field Effect Transistor(MOSFET) driver circuit controlled using the DSP processor.

The overall circuit is marked into different parts which comprises the complete SAPF setup for the experimentation. The portion marked as “three phase transformer” is linked to with the three-phase supply output as discussed which steps down from 415V to 140V. The printed circuit board (PCB) board marked as DSP-TMS320F28335 is the DSP controller that is used to develop the Pulse width Modulation (PWM) for the SAPF, which is the three level three phase inverter by observing the voltage and current from the three phase grid. Voltage and the current sensors with the signal processing units are used to generate the voltage and current sensed inputs to the DSP controller. The sensed voltage and current provided to the analog to digital converter (ADC) of the DSP is accepted in the MATLAB co-simulation and PWM generation happens from the MATLAB and is targeted on the DSP processor.

The PWM signals are developed from the DSP processor controlled from the SPWM control using the d-q control method for grid synchronization method which senses the voltage and current from both the inverter and the three phase transformer. The PWM thus generated is used to trigger the MOSFETS of three phase three level inverter in order to reduce harmonics with the three phase transformer output. The pulses which are generated from the DSP processor are fed to the MOSFET through the buffer and Optocoupler. The driver circuit highlighted in the experimental setup comprises of “CD-4050 Buffer”, “OPTO coupler”, and “MOSFET Driver IR2101” respectively. The DC input side of this circuit comprises of the auto-transformer and the DC link with the rectifier. The capacitors are rated for 200V which can withstand 140V peak desired for the inverter output at the PCC.

The three-phase output connection from the inverter output is connected to the voltage and the current sensor circuits that would generate the reference for the dq controller. The sensed voltage and current observed from the inverter output are passed through the clipping and clamping circuits. The output of the clipping and clamping circuits are given as the input to the ADC of the DSP processor.

The three-level inverter has power by the direct-current link capacitor. supplying the three-phase, three-level inverter that is connected to the DC link’s output via a capacitor. In order to further manage the DC link voltage and the power regulation at the grid side inverter, the DSP processor (TMS320F28335) employs voltage and current detectors to get the voltage, current, and DC link voltage at the grid. In DSP processor, the unidirectional ADC output is given by means of the clipping and clamping circuit. 230V/12V transformer with 1 ampere rating transformer is used for sensing the grid voltage.The voltage and current measured in the implementation need the signal to the processors . But the processor can’t receive the negative voltage since the signal processing can be done with the positive peak voltage. This leads to the use of both the clipping and the clamping circuits. The clipping circuit is a half bridge rectifier circuit that cuts off the negative portion of the sensed voltage and current circuit. A straightforward diode circuit is used for clipping, while an amplifier circuit is used for clamping. This circuit for clipping and clamping is

one of the system's key protection circuits. The immediate connection of detected signals to the ADC is made possible by the clamping circuit, which pushes the negative half cycle to the positive part of the waveform.

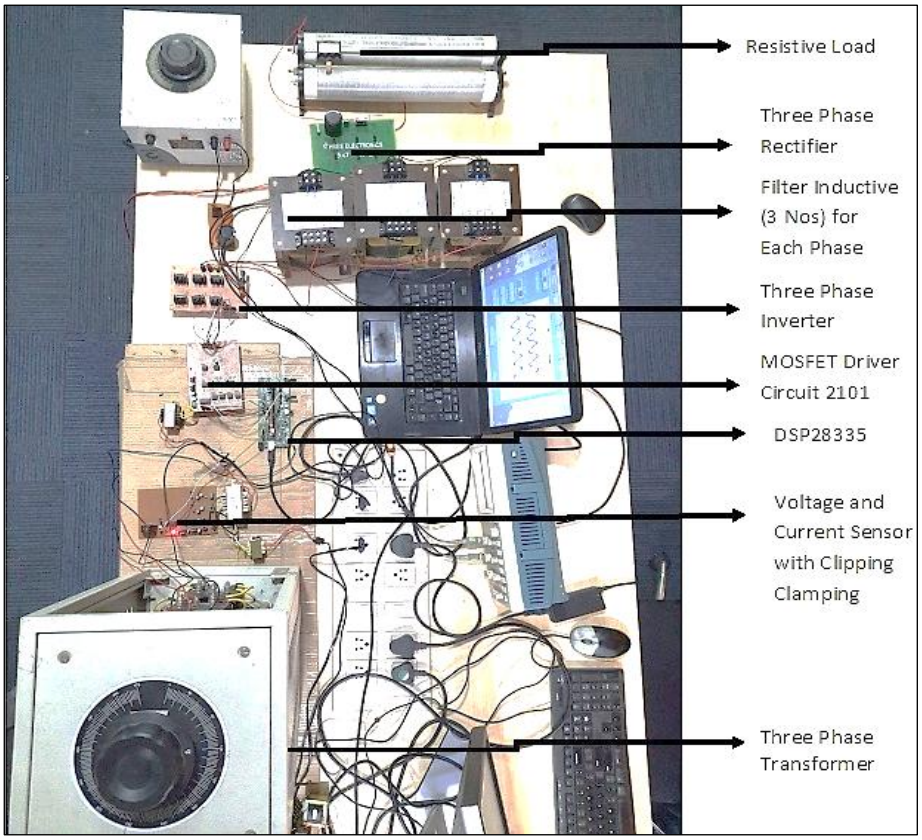

Figure 5: Experimental Setup-Schematic of the System

Hardware Design

Current Sensor: The SAPF algorithms require real-time voltage and current measurements, hence a current sensor is employed. Ohm's law would also be used to determine the current after measuring the voltage decreases across the shunt resistor. However, the voltage loss would be extremely modest due to the little resistance. A sensor circuit is utilized since the current controller was unable to detect such low levels. Figure 6 shows how to use a current sensing circuit to increase the voltage drop that is received through the ADC. The voltage divider equation [1] defines the calibration equations for this sensor circuit.

$$V_{out} = I_{in} R_{short} \frac{R_{out}}{R_{in}} \qquad [1]$$

Where R_{shunt} = 0.008Ω. Since the current is analog, the input voltage can have a maximum input as 5 V. The equation 1 becomes,

$$5 = I_{in} 0.008. \frac{R_{out}}{R_{in}} \qquad [2]$$

In addition, R_{in} was selected as 800Ω and R_{out} as 250kΩ. As a result, the design takes into account the maximum current and resolution, and 5 V input voltage equals 2.5 A and 0.05 V equals 0.025 A.

Voltage Sensor: Figure 7 illustrates the construction of a basic voltage divider used to measure the input voltage. A circuit that uses a voltage divider reduces the voltage so that the ADC can measure it. The voltage divider circuit is able to calibrate the voltage variation in the circuit because the sensor can only monitor up to 5 V.

The expression for the output voltage derived from Ohm's law is

$$U_{out} = U_{in} \frac{R_2}{R_1 + R_2} \qquad [3]$$

Equation [3] would produce a matching scale because it can read up to 5 V, and the values of R1 and R2 were selected to be large. Both the generator's output and the inverter's input use the voltage splitter.

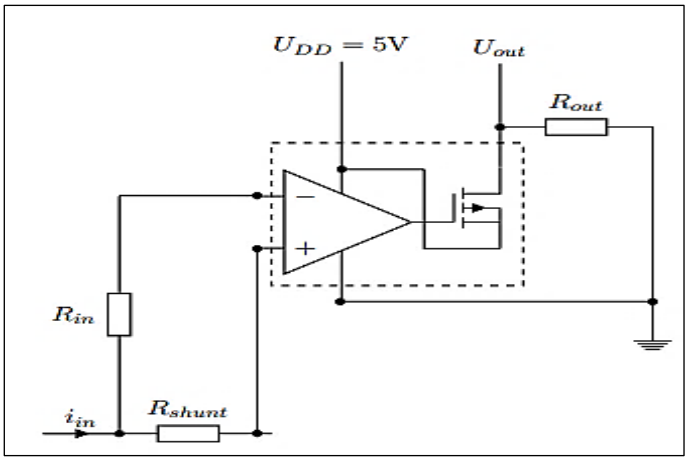

Figure 6: Circuit Diagram of Current Sensor

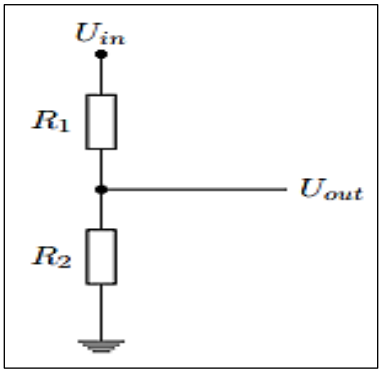

Figure 7: Schematic Diagram of Voltage Sensor

Clipping and Clamping Circuits: Depending upon the compatibility of the ADC, The DSP processor is designed to accept only positive voltage levels within the range of 0 to 3.3/5V with the help of clipping and clamping circuits, as shown in figure 8 and figure 9. The AC waveform is fed back to the controllers via these circuits. By clipping the restricted voltage and the circuit restricts the offset of the alternating current voltage, thereby guaranteeing that the voltage and current readings at the grid remain within the specified limit of 0 to 3 volts.

Here, the voltage from the sensor is given to the DSP. The clamper circuit is used to convert the alternating voltage from the sensor to the unidirectional voltage. The voltage level needs to be reduced to the voltage level within the 3V range.

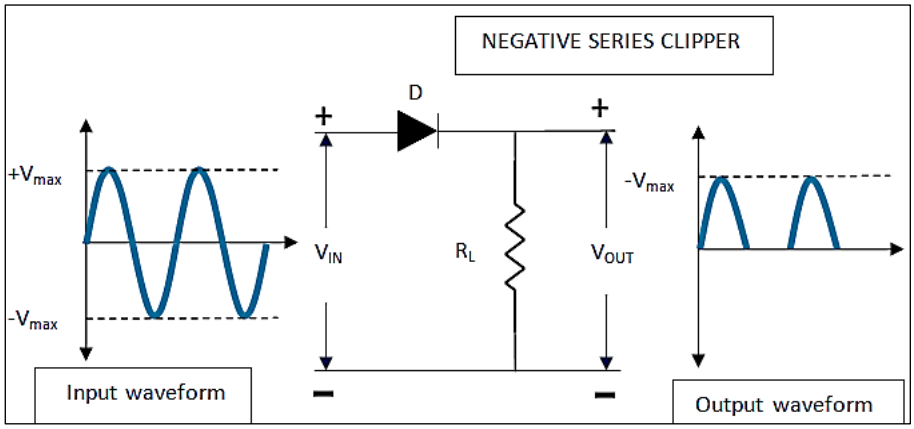

Figure 8: Circuit Diagram of Clipper

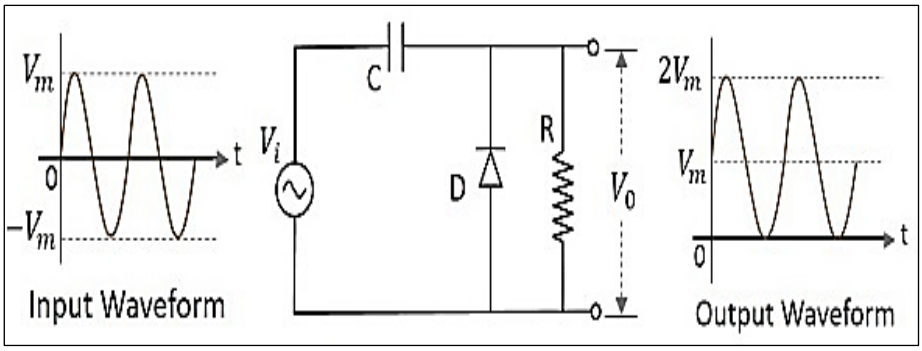

Figure 9: Circuit Diagram of Clamper

DSP Processor: Due to its many features, including modules such as ADC, Serial, and ePWM, plus its ability to utilize 150Hz as the chip frequency, the DSP TMS320F28335 is an excellent fit for this solution. Each module's specific requirements are outlined below. This DSP version is compatible with embedded coders based on MATLAB.

ADC Module: A 12-bit pipelined analog-to-digital converter (ADC) is the TMS320x2833x ADC module. Voltage regulators, sample-and-hold (S/H) circuits, front-end analog multiplexers (MUXs), the transformation core, and additional analog supporting circuits make up the converter's analog circuits; the term "core" refers to the core in this article. The programmable conversion sequencer, result registers, interfaces to additional on-chip modules, analog circuits, and device peripheral buses are all included. Here pin number of A0, A1 are used to measure the input voltage and current respectively through the help of voltage and current sensor. Then the V_{grid} and I_{grid} values are measured by sensors and treated by the clip clamp circuits before connecting to the ADC channels A2 and A3 respectively.

Enhanced Pulse Width Modulation (ePWM) Module: Complex pulse width waveforms must be produced via an efficient PWM peripheral with little assistance or CPU overhead. It must be simple to use and comprehend, highly programmable, and versatile. These needs are met by the ePWM unit presented here, which allocates the necessary timing and control resources according to each PWM channel. The smaller single channel modules that make up ePWM have separate resources and can cooperate to form a system when necessary, avoiding cross coupling or resource sharing. With an orthogonal manner and a clearer perspective of the marginal configuration, this modular approach makes it easier for users to rapidly comprehend how it works.

The Sinusoidal Pulse Width Modulation (SPWM) pulses generated from the dq controller is fed to the grid side controller through the ePWM numbered 00 to 11 pins to get harmonic reduction with the grid with the DC link voltage regulation.

Serial Communication Module: The Serial Communications Interface (SCI) is a two–wire asynchronous serial port, commonly known as a Universal Asynchronous Receiver/Transmitter (UART). The standard Non-Return-to-Zero (NRZ) format is used by the SCI segments to facilitate digital communications among the CPU and other asynchronous peripherals. Each SCI receiver and transmitter has its own distinct enable and interrupts bits and uses a 16-level deep first-in, first-out (FIFO) system to minimize service overhead. For half-duplex communication, both can be used separately; for full-duplex communication, both can be used simultaneously. The Simulink based embedded coder is connected to the DSP processor through the serial port while programming.

The ADC reading which acts as the rest of the steady state model in the MATLAB. Here, the Fuzzy rule is embedded into the DSP Processor. The Simulink model also shows the phase lock loop (PLL) module depicted as "V_{grid}, I_{grid} ADC read" is the DSP interface, where the angular phase locking is generated for the voltage waveform. The PLL module provides the instantaneous phasor angle to the decoupling module which generates the orthogonal coordinates of the phase voltages. Thus the complete dq controller algorithm is developed. The Figure 10 depicts the overall hardware in loop rapid prototyping implementation using embedded coder.

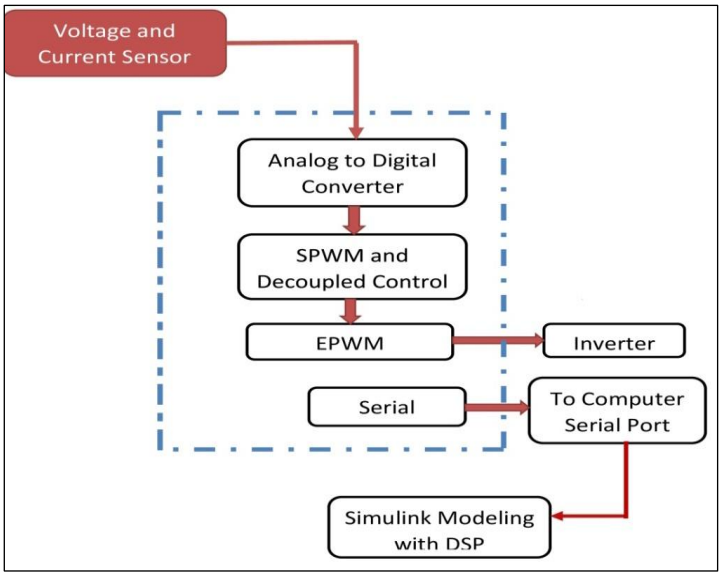

Figure 10: Overall Block diagram – SAPF Emulation Using Hardware in Loop (HIL) Implementation Using MATLAB

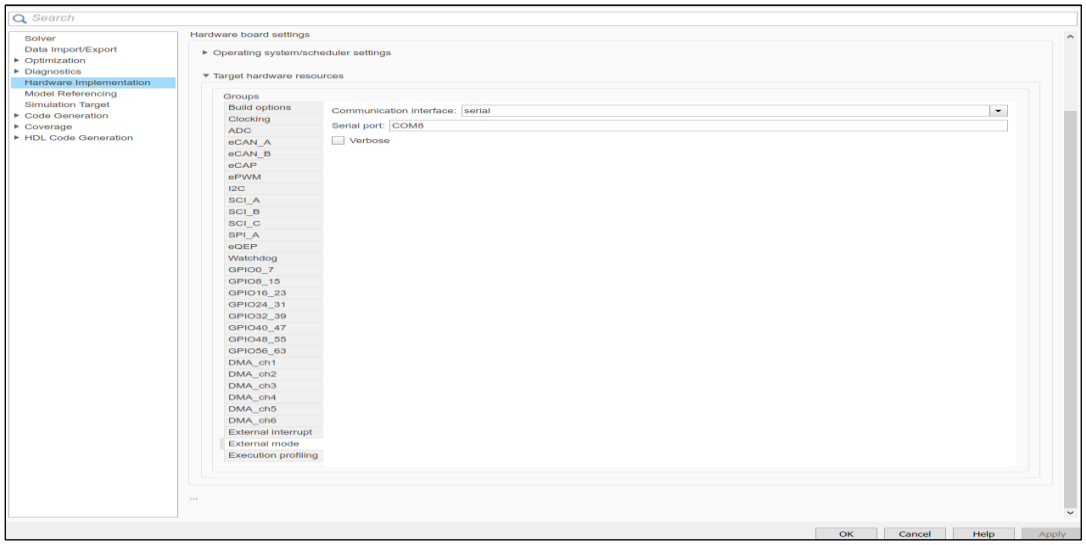

Figure 11: Hardware Implementation External Mode in COM8

The ADC input obtained in the DSP is interfaced with the Simulink model. The complete SAPF with Fuzzy Controller is simulated according to the scaled down parameters and the complete controller portion is targeted on the DSP such that the hardware. Hardware implementation external mode in COM 8 port is shown in Figure 10. ADC receives the sensor inputs and carries on the control for the hardware connected to the DSP. The ePWM section supplies the inverter switches from the DSP. The hardware setup for Fault Detection is shown in the Figure 11. The fault classification of the harmonic power quality is found by the Neuro-Fuzzy controller and the result is obtained from the ePWM controller. The fault detection is carried out for the series compensation issue by providing the non-linear load in the load side of the supply.

Results and Discussion

The three-phase rectifier is connected to the circuit at the particular time between 30 to 33 Secs and the harmonic fault is obtained in the Figure 10. The fault classification of the harmonic power quality is found by the Neuro-Fuzzy controller and the result is obtained from the ePWM controller. The fault detection is carried out for the series compensation issue by providing the non-linear load in the load side of the supply. The three-phase rectifier is connected to the circuit at the particular time between 30 to 33 secs and the harmonic fault is obtained in the Figure 12.

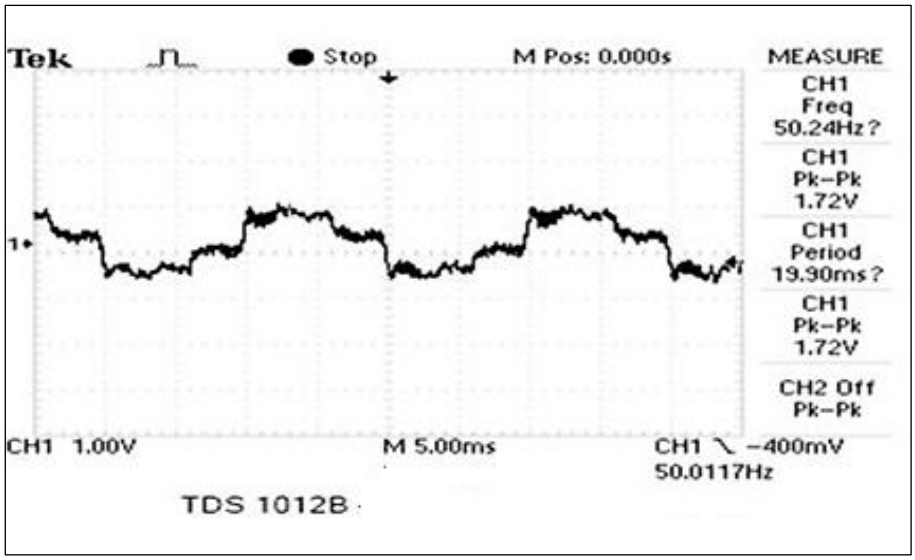

Figure 12: Real Time Fault Detection Output from DSP ePWM Pins for Harmonics Fault

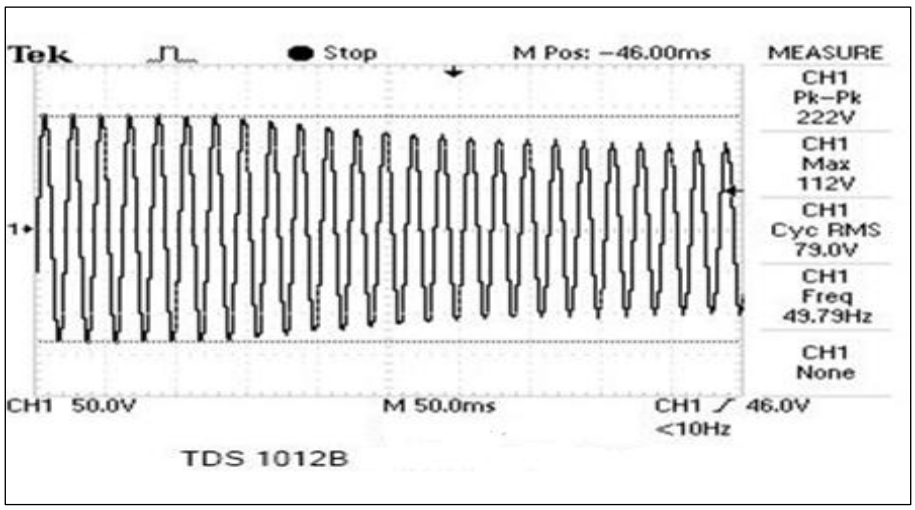

Figure 13: Real Time Fault Detection Out from DSP ePWM Pins for Sag Fault

The sag fault is introduced in the system by increasing the load by adjusting the rheostat. The output of the DSP controller after classifying the output from the ePWM pins for the sag fault is as exposed in the Figure 13.

The interruption of the power is obtained by removing the supply to the load which is sensed by the voltage and current sensor and the classifier classifies it as the interruption fault .The obtained output ePWM is shown in the Figure 14.

The three phase supply connected to the three phase rectifier provides the current waveform with the harmonics as shown in Figure 15.

The Voltage and current waveform at the load side is joined with nonlinear load. The harmonics involved in the current waveform is displayed in Figure 16. The deadbeat in the current waveform clearly shows that the harmonics in current waveform.

The SAPF output would reduce the harmonics and the obtained source side voltage and current is displayed in the Figure 15. The current waveform is sensed at the source side with mitigation of harmonics and removal of deadbeat. SAPF compensated voltage and Current at source side, the voltage for A and B phase with the phase shifted and the source side voltage for the Phase B and Phase C are displayed in Figure 17, 18 and 19.

To attain the nonlinear load output, the three Phase Transformer output is directly connected to the three phase rectifier. The three phase rectifier introduces the non-linearity to the source and the harmonics are introduced in the system. This system would provide the harmonics to the system. The THD is obtained from the SAPF before the shunt compensation.

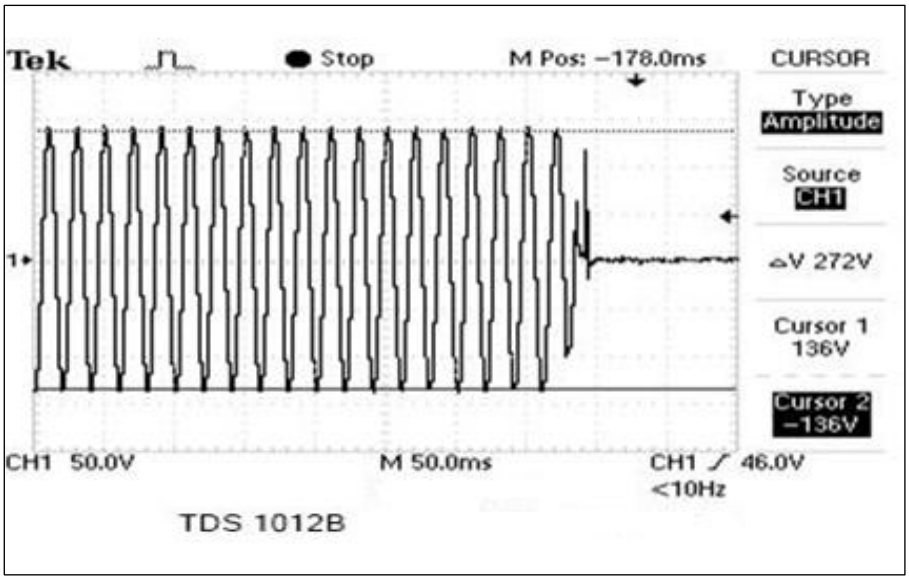

Figure 14: Real Time Fault Detection from DSP ePWM Pins for Interruption Fault

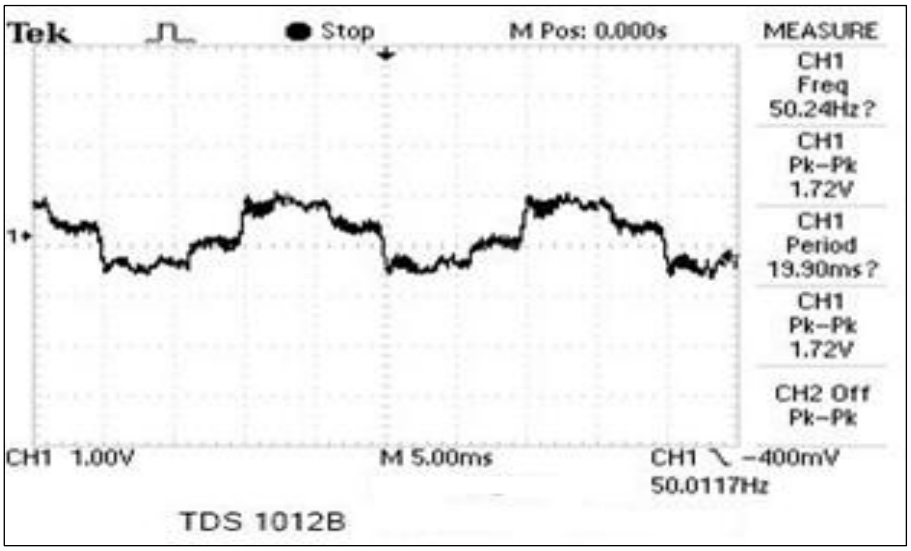

Figure 15: Rectifier Load Harmonics Response in Current (Phase A)

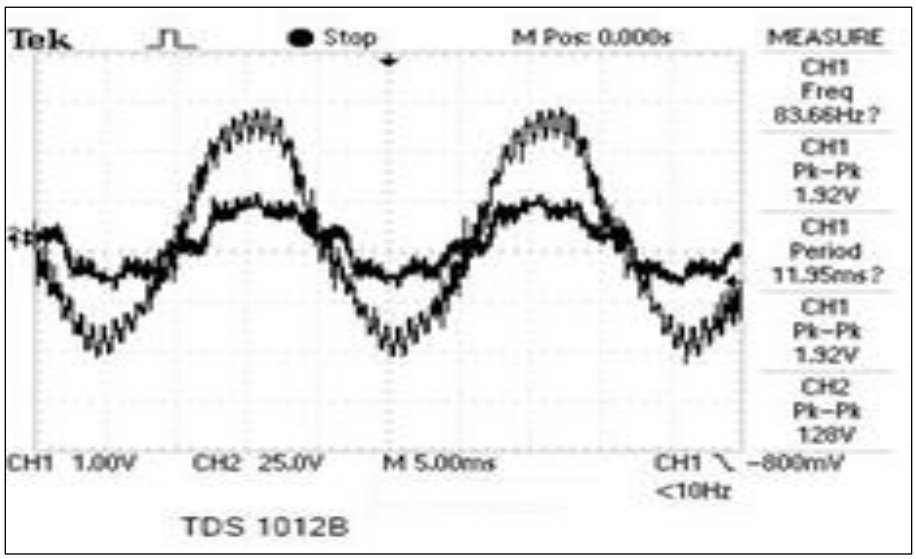

Figure 16: Voltage and Current with Nonlinear Load (Rectifier Load)

Using a fuzzy logic controller, a shunt active filter is fitted in the three-wire, three-phase system with a non-linear load to lower the current harmonics. For nonlinear loads, FLC is utilized to regulate the shunt active filter when the source voltage is balanced. To keep the load current sinusoidal and the dc link voltage constant, FLC controllers are designed to improve system comprehension. This was accomplished by comparing the system's fuzzy logic controller with one another. The filter circuit sends a control signal to the load based on this outcome.

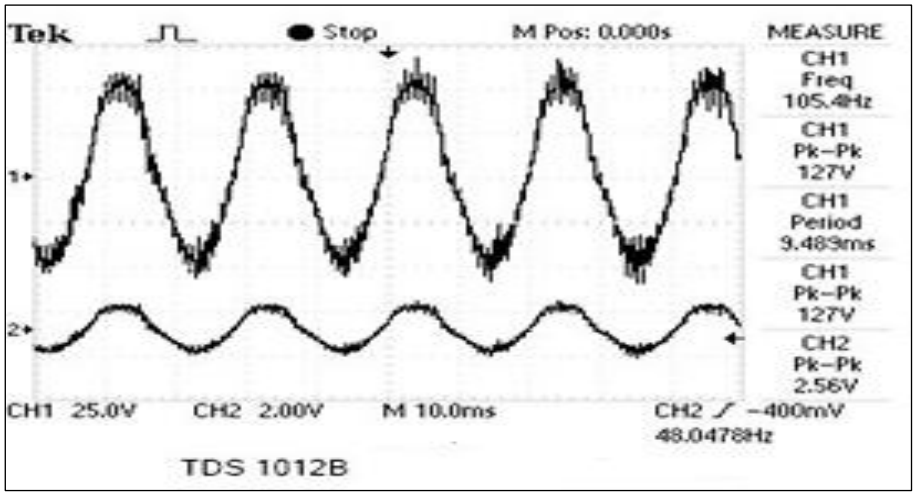

Figure 17: SAPF Compensated Voltage and Voltage at Current at Source Side

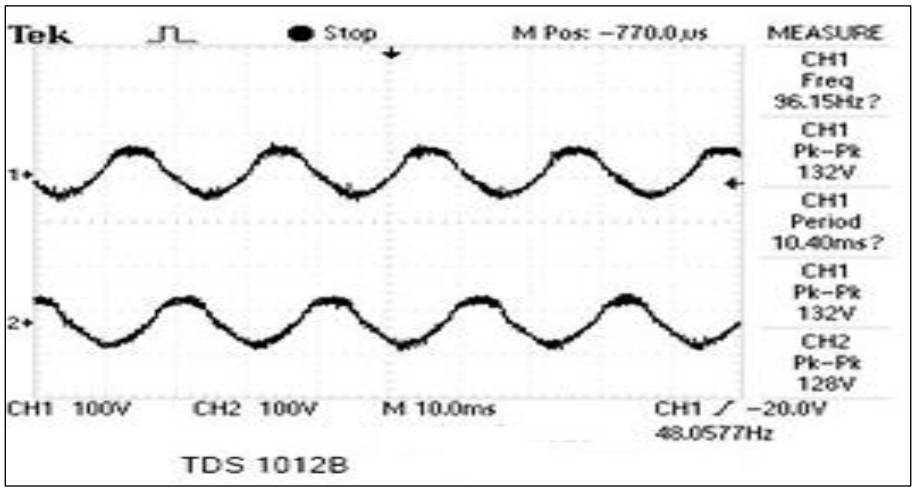

Figure 18: Phase A and B Source Side

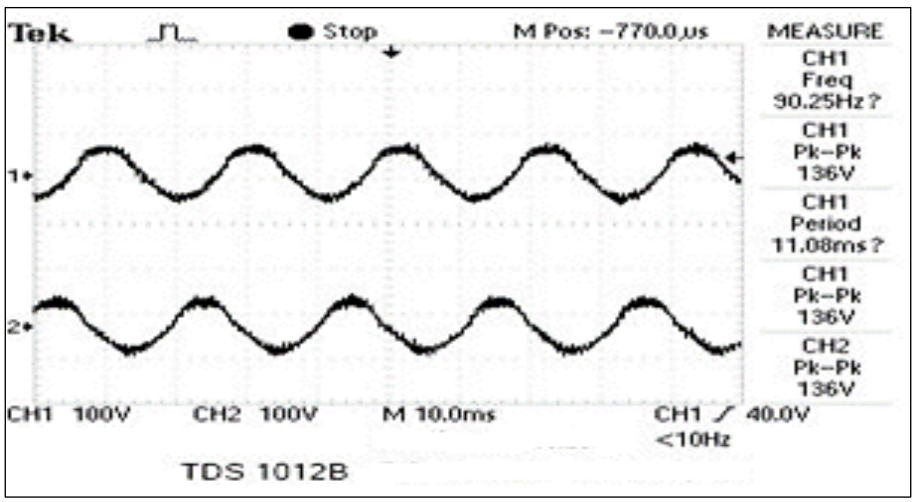

Figure 19: Phase B and C Voltage at Source Side

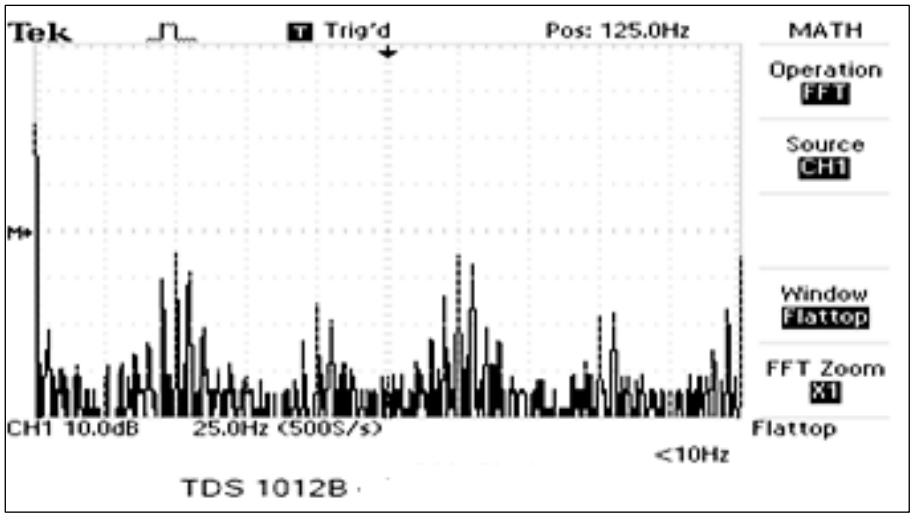

Figure 20: THD obtained with Harmonics

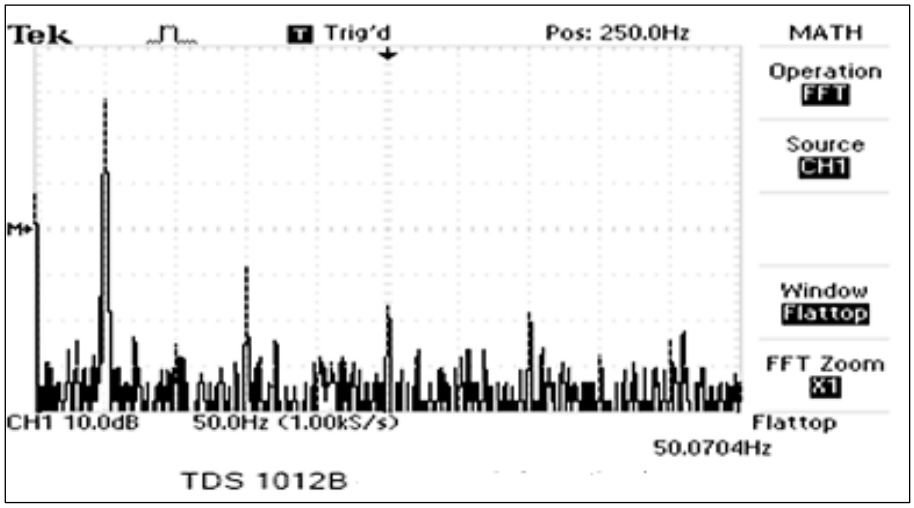

Figure 21: THD obtained after Compensation

Figure 20 shows the Fast Fourier Transform (FFT) output from the Digital Storage Oscilloscope (DSO) when the three phase rectifier is connected to the three phase transformer. Current waveform is measured and the results are obtained with harmonics. From the observed result, before compensation the THD value is 23 %. The compensated current after SAPF using FFT is displayed in the Figure 21. It can be detected that the amplitude of the 50Hz component is high in the compensated FFT. Here, THD value is 4.3 %. The overall implementation of the hardware using Fuzzy algorithm is found to be satisfactory.

Conclusion

In this work, the fuzzy controlled SAPF with DSP28335 controller is carried out. Once the faults are detected from this technique, the compensation can be done using the closed loop implementation. Here the shunt compensation can be extended to series compensation also. The DSP processor is compatible for the real time implementation of the compensation. The current compensation is clearly evident in the hardware model and can be extended for the series compensation. Both the fault classification and the SAPF for shunt compensation are carried out using the DSP controller and results are found to be satisfactory. The NFS approach has the ability to categorize power quality disturbances performance efficiently and accurately. The present work may be extended by applying signal processing techniques like frequency spectrum estimation techniques for feature extraction. The proposed signal processing algorithms will be implemented using VLSI processors for real-time applications. Also, other ANN architectures like Adaptive Resonant Theory (ART) and Support Vector Machine (SVM) may be explored for automatic disturbance classification. The power

quality disturbance waveform will be generated by using power system analysis tools such as Electromagnetic Transient Program (ETP) and Alternate Transient Program (ATP). Further, real-time disturbance signals will be collected from real power system. Digital signal Processor (DSP) will be used for capturing and processing the disturbance waveforms.

Abbreviations

CHB: Cascaded H-Bridge, DSO: Digital Storage Oscilloscope, DSP: Digital Signal Processor, ePWM: Enhanced Pulse Width Modulation, EZ-Easily, FC: Flying Capacitor, FFT: Fast Fourier Transform, FIFO: First-in First-out, FLC: Fuzzy Logic Controller, GaN: Gallium Nitride, IGBT: Insulated-Gate Bipolar Transistors, MOSFET: Metal Oxide Semiconductor Field Effect Transistor, NB: Negative Big, NFS: Neuro Fuzzy System, NM: Negative Medium, NRZ: non-return-to-zero, NS: Negative Small, PB: Positive Big, PCB: Printed Circuit Board, PCC: Point of Common Coupling, PI: Proportional Integral, PLL: Phase Locked Loop, PM: Positive Medium, PQ: Power Quality, PS: Positive Small, PWM: Pulse Width Modulation, RES: Renewable Energy Sources, SAPF : Shunt Active Power Filter, SCI: Serial Communications Interface, SiC: Silicon Carbide, SPWM: Sinusoidal Pulse Width Modulation, THD: Total Harmonic Distortion, UART: Universal Asynchronous Receiver/Transmitter.

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Author Contributions

All Authors contributed the entire manuscript in writing, reviewing, implementing, Conceptualization and Analysis.

Conflict of Interest

The authors declare that they have no conflicts of interest.

Ethics Approval

This research did not involve human or animal subjects; therefore, ethics approval is not applicable.

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