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A Compact and Power-efficient X-band PLL for High-frequency Wireless Communication in 45 nm CMOS

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Abstract

A low-phase-noise X-band Phase-Locked Loop (PLL) designed for advanced wireless communication systems, such as satellite communications, 5G/6G networks and millimeter-wave applications, is presented in this paper. Designed in 45 nm CMOS using Cadence, the PLL integrates a high-performance varactor-based Voltage-Controlled Oscillator to achieve superior frequency tuning and phase-noise performance. The architecture supports a wide frequency range of 8–12 GHz, suitable for X-band operation and is driven by a 125 MHz reference with a programmable division factor (N = 64–96), offering flexibility across various wireless platforms. The Phase-Locked Loop achieves a phase noise of -104.05 dBc/Hz at a 1 MHz offset, ensuring signal integrity and spectral purity critical in densely packed wireless environments. Featuring a compact footprint and power-efficient design, the proposed system consumes only 9.6 mW and achieves a Figure of merit (FoM) of −161.35 dBc/Hz, making it highly suitable for portable and battery-powered applications. This implementation demonstrates a highly integrated, economical solution for high-frequency communication, offering enhanced stability, low jitter and low power consumption. The proposed PLL meets the growing demands of modern wireless infrastructure, where high data rates, frequency agility and low noise performance are essential for reliable and scalable system deployment.

Keywords: CMOS, High Frequency, Low Phase Noise, Varactor-Based VCO, X-Band.

Introduction

The increasing demand for high-speed wireless communication, radar sensing and satellite systems has driven the development of high-frequency and low-noise frequency synthesis techniques. In modern radio-frequency and millimeter-wave communication systems, Phase-Locked Loops play a critical role in generating stable and accurate local oscillator signals required for modulation, demodulation and clock synchronization. Particularly, the X-band frequency spectrum (8–12 GHz) is widely utilized in radar systems, satellite communication links and emerging high-data-rate wireless networks due to its ability to support high bandwidth and reliable signal propagation. A PLL is a feedback control system that synchronizes an output signal's frequency and phase with a reference signal. A phase-frequency detector (PFD), charge pump (CP), loop filter (LF), voltage-controlled oscillator (VCO) and frequency divider make up the basic PLL architecture. The output frequency of a PLL can be expressed by using Equation [1], where the output frequency is determined by the multiplication of the reference frequency and the division factor within the feedback loop. Therefore, improving VCO performance while maintaining low power consumption and stable loop dynamics is essential for achieving efficient frequency synthesis in RF systems.

$$F_{out}=N\cdot F_{Ref} \quad [1]$$

Where, F_{out} is the output frequency, F_{Ref} is the input reference frequency and N is the division factor in the feedback loop.

Various studies have provided insights into PLL architectures, voltage-controlled oscillator design with varactor tuning and phase-noise optimization techniques for developing high-performance frequency synthesizers (1). With benefits like digital compatibility, lower power consumption and small chip footprint, CMOS-based integration is extensively used and enhances system

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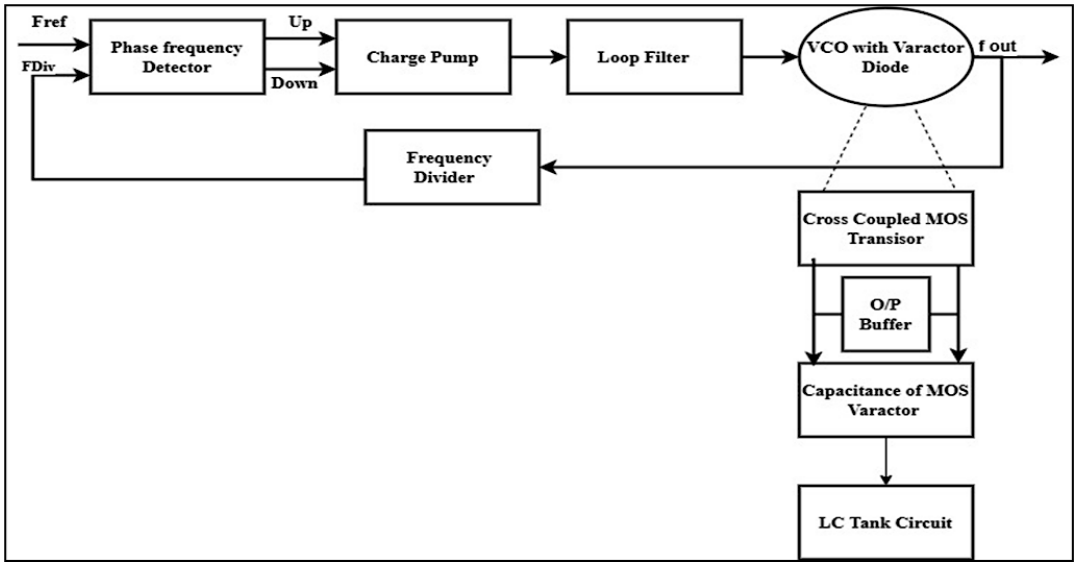

Figure 1: Block diagram of the proposed PLL with a varactor-based Voltage-Controlled Oscillator

performance in applications like satellite communication and the upcoming 5G networks (2). The reduced device size achieved minimizes fabrication cost and chip area while enabling efficient integration of RF and digital circuits within a single platform (3). Advanced control approaches such as sliding-mode control have also been investigated to suppress dead-zone effects in nonlinear dynamic systems, thereby improving system stability and response accuracy (4-6). To achieve these requirements, several VCO architectures have been proposed to improve tuning range and phase noise performance (7, 8).

MOS-varactor-based VCO structures have been extensively studied to enhance tuning range and phase noise performance in high-performance frequency synthesizers (9-11). Improvements in phase-frequency detector architectures have been proposed to enhance PLL performance (12-14). PLL techniques have also been extended to power-quality applications, where frequency-adaptive PLL structures are used for harmonic compensation in single-phase inverter systems (15, 16). Figure 1 illustrates the architecture of the proposed PLL system used in this study. The system consists of a phase-frequency detector, a charge pump, a loop filter, a voltage-controlled oscillator and a frequency divider. In this configuration, a cross-coupled MOS structure with varactor tuning controls the LC tank circuit of the VCO, while the feedback loop stabilizes the oscillator frequency and synchronizes it with the reference signal.

At X-band frequencies, device parasitic effects, substrate noise coupling and reduced transistor gain significantly affect oscillator stability and loop dynamics (17). Many PLL systems currently in use either operate at higher frequencies with higher power consumption or focus on achieving extremely low phase noise at lower frequencies. Additionally, deep-submicron CMOS technologies provide challenges like reduced inductor quality factors, increased process fluctuations and nonlinear varactor properties that might impact overall PLL performance. These limitations highlight the need to improve PLL architectures capable of operating frequency within the X-band region while maintaining compact design and low power consumption (18). Another challenge is the nonlinear behavior of the charge pump and phase-frequency detector circuits, which can lead to phase errors and a rise in reference spurs. Reduced spectral purity may arise from dead-zone effects in PFD operation, which can create phase errors and increase reference spurs. Similar to this, nonlinear capacitance variation in MOS varactors can lead to differences in VCO gain, which have an immediate effect on phase noise performance and loop stability. Given these difficulties, there is still a research gap to develop compact X-band PLL architectures that use contemporary CMOS technology to simultaneously achieve low phase noise, a large tuning range and low power consumption. Closing this gap is crucial to enabling high-performance RF front-end circuits that are necessary for next-generation communication

systems. Specifically, combining optimized varactor-based VCO architectures with robust loop filters and efficient phase-frequency detectors can significantly improve PLL performance at GHz frequencies.

The proposed design incorporates a varactor-based voltage-controlled oscillator, optimized charge pump and loop filter and stable PFD architecture to achieve reliable frequency synthesis across the X-band range (19). This work's particular targets are to assess overall system performance via cadence RF simulation, improve phase noise characteristics through optimized VCO tuning and analyze loop dynamics for high-frequency operation.

The novelty of the proposed work lies in the integration of a varactor-based VCO with optimized loop dynamics in a compact 45 nm CMOS PLL architecture (20). The suggested design offers an effective solution for modern high-frequency communication systems that require compact, low-noise and power-efficient frequency synthesis by integrating theoretical simulation with RF simulation techniques, including periodic steady-state and phase-noise analysis.

Methodology

The reference signal $F_{ref}$is compared with the divided output F_{div}using a conventional D flip-flop-based PFD structure, which generates UP and DOWN control pulses proportional to the phase and frequency difference. Phase error is converted into current pulses by a current-steering charge pump driven by these pulses. The charge pump output is passed through a passive second-order loop filter composed of R_1, C_1 and C_2, generating a control voltage V_{ctrl}. The filtered control voltage tunes the LC-VCO through accumulation-mode MOS varactors, enabling fine frequency tuning around the center frequency. The LC tank formed by inductors L_1, L_2 and varactors determine the oscillation frequency. To preserve oscillation and mitigate tank losses, a cross-coupled transistor pair offers negative resistance.

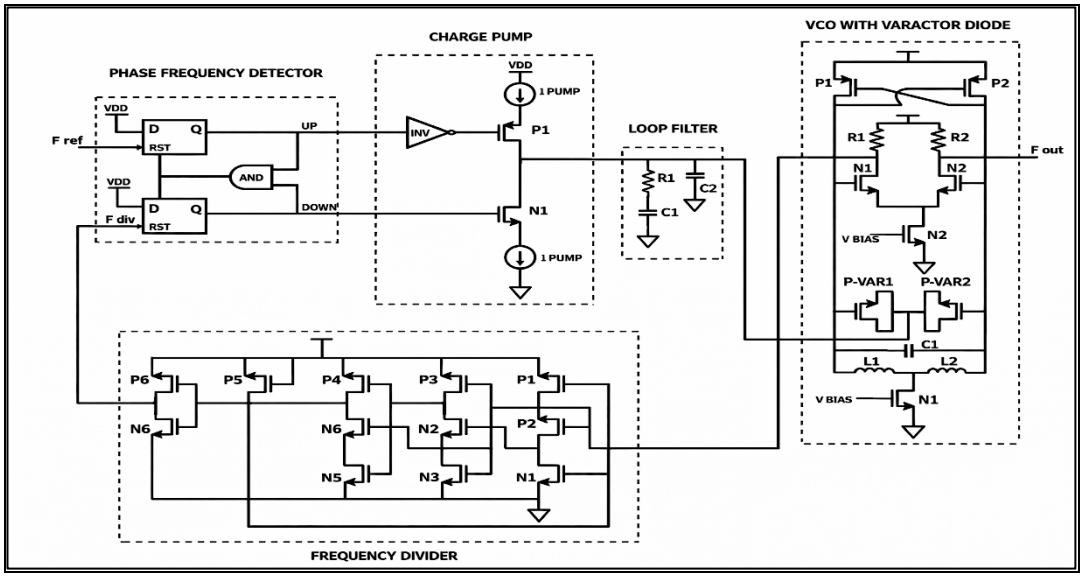

Figure 2: Proposed PLL Schematic Diagram with Varactor-based VCO Phase Frequency Detector

A Phase-Locked Loop comprises multiple interconnected functional blocks that work together to synchronize the output signal with the reference signal. The proposed Phase-Locked Loop with a varactor-based VCO with PLL schematic is presented in Figure 2. The output frequency, which is controlled by the control voltage, is produced by the VCO with a varactor diode. For feedback, the VCO output is scaled down using a frequency divider. For high-frequency applications, this design guarantees low phase noise and steady frequency generation. In the linear region, the PFD produces output pulses proportionate to the phase difference between the divided feedback frequency and the reference frequency. It ensures precise phase comparison with its two D flip-flops and reset logic. To raise the VCO frequency, the PFD generates a UP signal and a DOWN signal (Figure 3) is produced in order to lower it by F_{div}. The PFD reduces jitter and ensures exact frequency locking in the PLL by providing a direct phase-error-to-voltage conversion within its linear

operating range, focused on using innovative PLL structures to improve lock time and reduce phase noise. In order to reduce time jitter and guarantee steady synchronization, these enhancements are essential. expanded on this work by creating a fractional-N PLL that greatly lowers jitter in mixed-signal settings by using voltage-domain quantization noise cancellation.

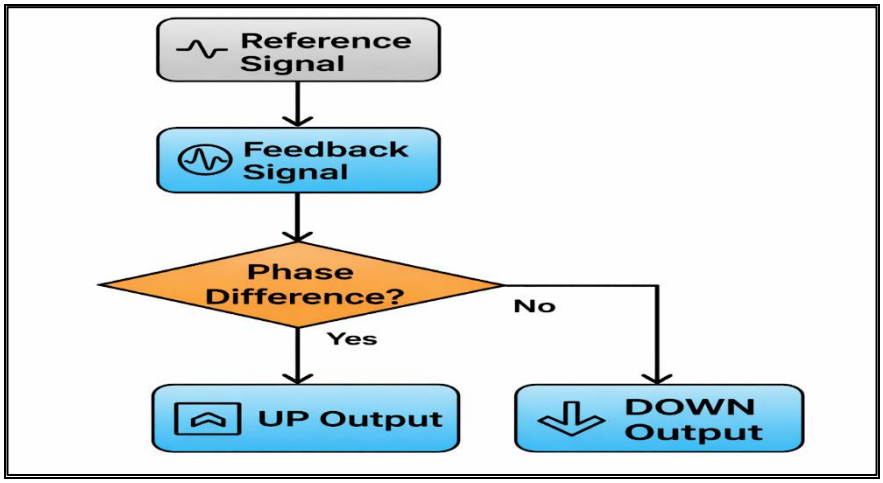

Figure 3: Flow chart for Phase Frequency Detector

In a PLL system, K is a constant that establishes a relationship between the frequency or phase of the input signal and the frequency or phase of the output signal. The K_{PFD} is calculated by dividing the pump current (I pump) by 2π, as given in Equation [2].

$$K_{PFD} = \frac{I_{pump}}{2\pi} \qquad [2]$$

Charge Pump with Loop Filter

The charge pump is actively dropping the VCO frequency by modifying the control voltage, as seen by the falling voltage trend in the Charge Pump & Loop Filter Output diagram. The Phase Frequency Detector is UP and DOWN pulses are correlated with the shifting, staircase-like pattern, which indicates periodic charging and discharging. The charge pump circuit's transient output voltage is represented in Figure 4 over time. The charging and discharging of the capacitors during switching cause periodic ripples in the waveform.

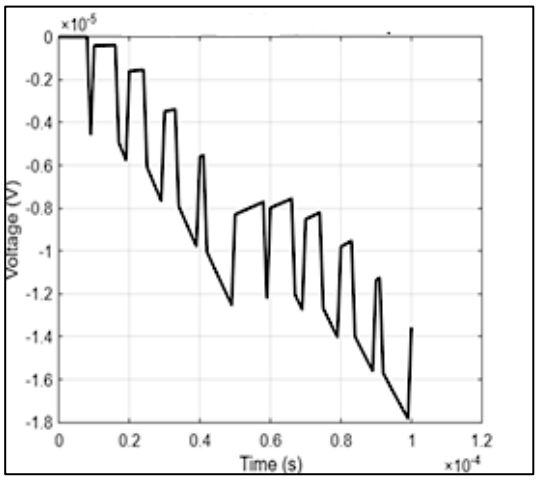

Figure 4: Time Domain Analysis of Charge Pump Output Voltage

Equation [3] may come from a PLL system in which the phase difference between two signals modulates the pump current. The output current may be normalized with respect to a parameter or averaged over time using Equation [4].

$$I(t) = Ipump \times (\Delta\emptyset(t)) \qquad [3]$$

$$= \frac{1}{C}\int_0^1 I_{out}(z)dz \qquad [4]$$

An active filter transfer function could be represented as Equation [5], where the frequency response is defined by the two capacitors and R1.

$$F(S)=\frac{1}{2\pi R_1 \frac{C_1 C_2}{C_1+C_2}} \quad [5]$$

Varactor-based Voltage-controlled Oscillator

Using a varactor diode, a varactor-based voltage-controlled oscillator adjusts the control voltage to achieve frequency tuning. Depending on the applied voltage, the varactor diode's capacitance changes, changing the VCO's oscillation frequency. By using a varactor, a small, low-power and extremely effective design is made possible, guaranteeing accurate and steady frequency modulation. It suggested a wide-tunable, low-power CMOS VCO with active inductors that provides tunability and energy efficiency. Similarly, a low-power VCO with a MOS varactor was built with the goal of employing as few transistors as possible for compact IC integration (21). Highlighted the significance of intelligent algorithms in analog design automation by using a multi-objective Salp Swarm Algorithm (SSA) to optimize a current-starved VCO, balancing phase noise and tuning range and utilizing Particle Swarm Optimization (PSO) for CMOS ring VCO design. expanded the operating bandwidth for VCOs by introducing a high-Q active inductor-based (22, 23). It demonstrated strong spectral purity and achieved a 166% tuning range using high-quality off-chip inductors. At centered on PLL-integrable, energy-efficient VCOs that improve system power profiles overall (24, 25).

Following the expected structure in Voltage-Controlled Oscillators caused by the filtering effect of the PLL loop, the VCO Phase Noise at Different X-Band Carrier Frequencies Figure demonstrates that phase noise improves as the offset frequency increases. Better phase noise performance is also seen at higher carrier frequencies; the 12 GHz signal has the lowest phase noise, followed by 10 GHz and 8 GHz. In Figure 5, the graph indicates that as offset frequencies increase, phase noise improves and decreases with higher VCO frequencies (8 GHz, 10 GHz and 12 GHz).

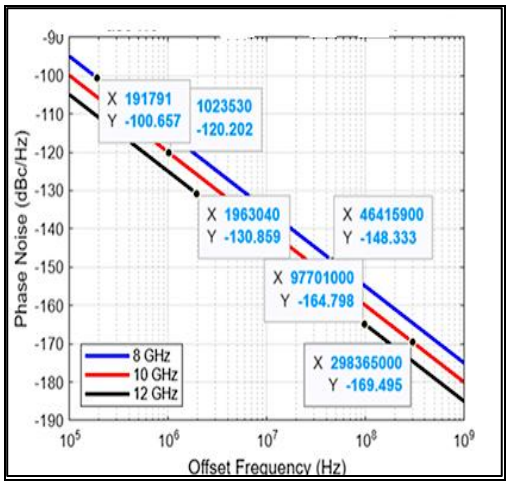

Figure 5: VCO Phase Noise at Different X-band Carrier Frequencies

$$f_{osc}=\frac{1}{2\pi\sqrt{LC}} \quad [6]$$

$$C_{var}=C_{max}\left(1-\frac{V_{ctrl}}{V^{th}}\right)^n \quad [7]$$

$$K_{VCO}=\frac{\Delta F_{out}}{\Delta V_{control}} \quad [8]$$

$$F_{out}=\frac{1}{2\pi\sqrt{L(C_{fix}+C_{var})}} \quad [9]$$

In an LC tank circuit based on inductance (L) and capacitance(C) for a frequency oscillator, with MOS varactor capacitance changes with control voltage and the sensitivity of the VCO output frequency to changes in the control voltage. The oscillation frequency of the LC oscillator is determined by the

inductance and capacitance of the resonant tank, as shown in Equation [6]. The varactor capacitance varies with the control voltage as expressed in Equation [7] $C_{var}=C_{max}$. The sensitivity of the VCO to the control voltage is defined by the VCO gain, as represented in Equation [8]. Equation [7] in turn controls the output frequency of the VCO given in Equation [9].

Frequency Divider

The frequency divider is composed of several CMOS logic gates, including flip-flop structures. The input frequency is reduced by a preset ratio thanks to these gates. Together, the PMOS and NMOS transistors in this device split frequencies efficiently while utilizing minimum power. Toggle flip-flops or sequential logic are most likely used in the circuit because each stage splits the frequency by two. Phase-locked loops, clock-generating circuits and radio frequency communication systems all make extensive use of this kind of frequency divider to offer reliable and synchronized signal processing. The entire architecture has an impact on system power efficiency, jitter performance and phase noise. Using the Laplace transform, the closed-loop transfer function of the PLL can be expressed as the ratio of the output frequency to the reference frequency, as shown in Equation [10]. The overall transfer function, including the phase detector, loop filter, VCO and frequency divider, is given in Equation [11].

Using Laplace Function:

$$H(S)=\frac{F_{out}(s)}{F_{ref}(s)} \quad [10]$$

$$H(S)=\frac{K_{pd}.F(S).K_{vc\emptyset S}}{1+(\frac{K_{PP}.F(S).K_{vco}}{SN})} \quad [11]$$

The PFD improves frequency acquisition through the elimination of phase ambiguity and offering a wide capture range. While the second-order loop filter adds a zero for better phase margin and guarantees loop stability, proper matching of the charge pumps UP and DOWN currents reduces steady-state phase error and reference spurs. Therefore, determining a suitable loop bandwidth is essential, as a smaller bandwidth decreases reference spur at the expense of higher integrated jitter, while an increased bandwidth suppresses VCO noise but increases reference noise coupling. A phase margin larger than 45° is confirmed by a stability study, guaranteeing quick locking with little overshoot. Whatever is considered, this proposed architecture successfully balances lock time, phase noise, power consumption and tuning range, making it appropriate for high-frequency wireless and Internet of Things applications

Results

The evaluation of the Phase-Locked Loop system performance is conducted using important characteristics such as power consumption, frequency range, phase noise and technology scaling.

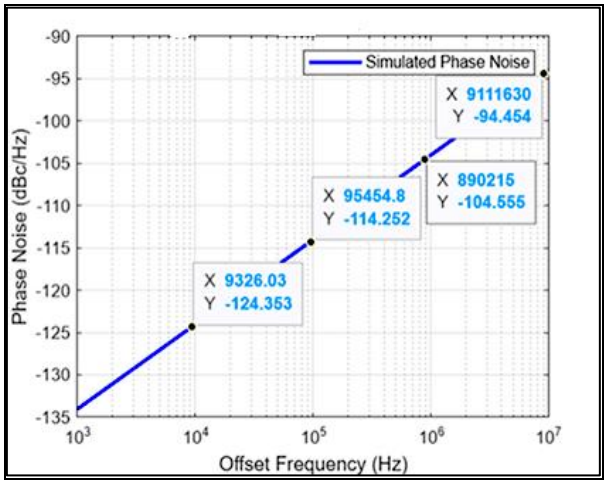

Figure 6: Phase Noise of X-band PLLA Across Different Offset Frequencies

According to the results, stable frequency synthesis and phase locking can be achieved by using the Phase Frequency Detector, Charge Pump, Loop Filter, Voltage-Controlled Oscillator and Frequency Divider, among other individual components. In Figure 6, the simulated phase noise of an X-band PLL is depicted and it decreases (increases) as the offset frequency rises from 10^3 Hz to 10^7 Hz. The simulated phase noise performance at different offset frequencies appears in the X-band PLL plots, Phase Noise Spectrum. As the offset frequency rises, the phase noise decreases, a common pattern observed in PLL systems. Phase noise is roughly -124.35 dBc/Hz at 9.3 kHz and deteriorates to -94.45 dBc/Hz at 9111 kHz. As the PLL output frequency approaches the desired 10 GHz, the lock transient response in Figure 7 shows comparable second-order loop dynamics with minimal overshoot.

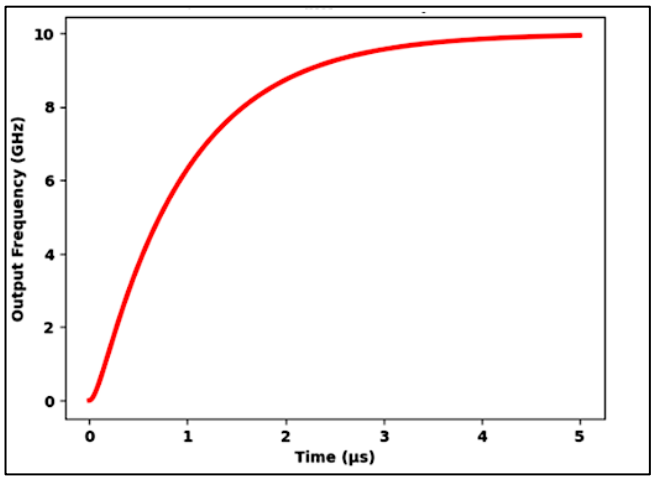

Figure 7: PLL lock Transient Response

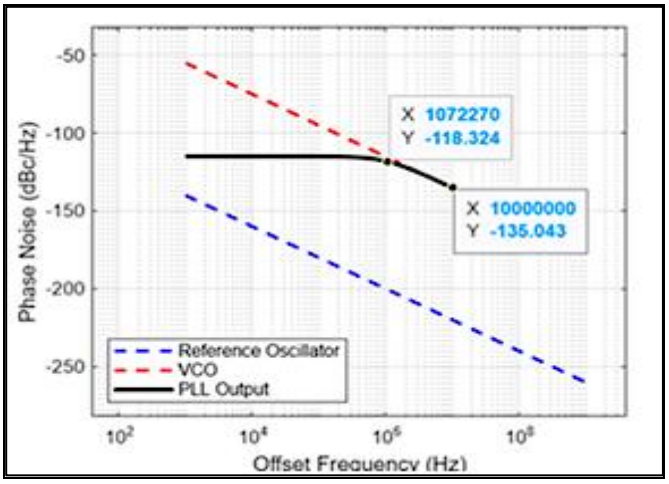

Figure 8: Phase Noise of Reference Oscillator, VCO, PLL

At greater offsets, the reference oscillator shows the least amount of phase noise, whereas the VCO displays more phase noise because of intrinsic oscillator noise. A more stable and low-noise signal is ensured by the PLL output, which efficiently suppresses the VCO noise at lower frequencies in Figure 8. The loop capacity to reduce phase noise at higher offsets is demonstrated by the phase noise, which is roughly -104.32 dBc/Hz at 1.07 MHz and improves to -135.04 dBc/Hz at 125 MHz.

Case (1) Output Frequency

$$F_{out} = N.freq$$
$$N = 96$$
$$F_{out} = 96 * 125MHz$$
$$= 12GHz$$

Case (2) Locking Condition

$$F_{in}\_out < \text{Lock Range}$$

Case (3) check stability (Damping factor)

$$0.5 \leq € \leq 1$$

In second & order Filter

$$\omega_n = \sqrt{\frac{I_{pump} K_{vco}}{N C_1}} \quad [12]$$

Case (4) Check Bandwidth (F_{BW})

$$F_{BW} = \frac{w_n}{2\pi} = \frac{1}{2\pi} \cdot \sqrt{\frac{I_{pump} K_{vco}}{N_{C1}}} \quad [13]$$

F_{BW} and compare with ref frequency

Case (5) PLL

$$H(S) = \frac{F_{out}(S)}{F_{ref}(S)}$$

$$H(S) = \frac{K_{pd}.F(S).K_{vco}/s}{1+(\frac{K_{pd}.F(S).K_{vco}}{S_N})} \quad [14]$$

Consider

F_{ref} = 125MHz

F_{out} = 10GHz

In Equation [1],

$$F_{out} = N \cdot F_{Ref}$$

$$N = \frac{F_{out}}{F_{ref}} = \frac{10 \times 10^9}{125 \times 10^6} = 80$$

Tuning range 8GHz to 12GHz

$$N = \frac{F_{out}}{F_{ref}} = \frac{12 \times 10^9}{125 \times 10^6} = 96$$

The PLL system's phase noise analysis shows how each component contributes at different frequency offsets. The phase noise at 1 MHz is roughly -80 dBc/Hz, demonstrating how well the system suppresses noise. Equation [12] calculates the second-order loop filter using the charge pump current, VCO gain, divider ratio and loop filter capacitance. Equation [13] expresses the loop bandwidth (FBW), which is derived from the PLL's natural frequency. Equation [14] provides the closed-loop transfer function of the PLL that describes the relationship between the output frequency and reference frequency. The reference oscillator, phase frequency detector, charge pump, loop filter and VCO are some of the causes of the total phase noise in Figure 9.

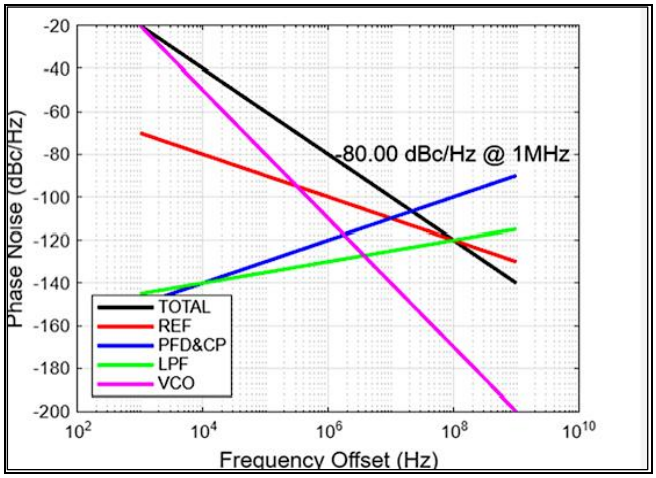

Figure 9: Breakdown of Phase Noise Contribution in PLL

Table 1 illustrates the better performance of the suggested 45 nm PLL for high-frequency wireless applications by highlighting important aspects, including technology node, frequency range, phase noise, power consumption and FoM. Plotting important PLL performance data reveals that, in comparison to current efforts, the suggested design achieves low phase noise, competitive FoM and low power consumption Figure 10.

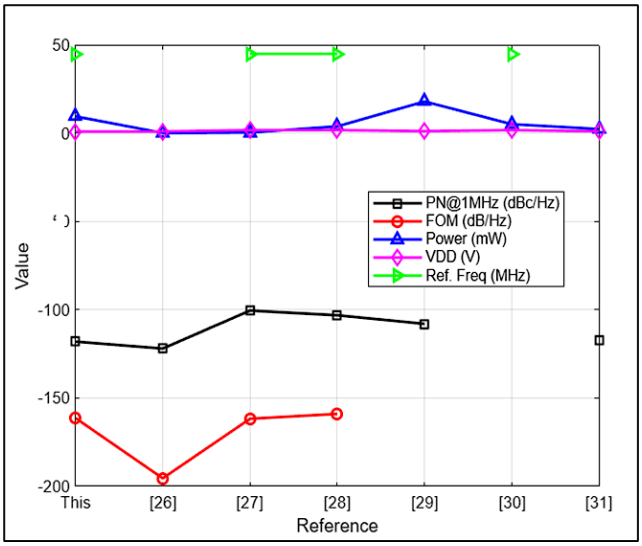

Figure 10: Comparison of Key Metrics PLL

Table 1: Comparison of State-of-the-art PLL Designs with the Proposed Work

Technology (nm)	Frequency Range (GHz)	Reference Frequency (MHz)	PN @1 MHz (dBc/Hz)	FOM (dB)	Power (mW)	VDD (V)	Reference
130	2–2.9	–	−122	−195.5	0.18	1	(26)
180	0.5–1.19	45	−100.45	−161.77	0.437	1.8	(27)
180	0.724–1.697	45	−103.1	−159	3.50–4.34	1.8	(28)
65	3–7	–	−108	–	18	1.2	(29)
180	1.06–3.731	45	–	–	5.15	1.8	(30)
180	2.94	45	−117.44	–	2.38	1.1	(31)
45	8–12	125	−104.05 −135.05@10MHz	−161.35	9.6	1	Proposed

With an emphasis on important characteristics such as technology node, supply voltage, frequency range, phase noise and power consumption, the comparison table displays the performance metrics of the suggested design in relation to previously published works. In Table 1, at low offset frequencies, the reference (REF) noise dominates the overall phase noise, while at high offset frequencies, the VCO noise does the same. With a reference frequency of 125 MHz, the suggested design, when implemented in 45 nm technology, achieves a frequency. It ensures low noise operation with a phase noise of -104.05 dBc/Hz at 1 MHz offset and -135.04 dBc/Hz at 10 MHz offset. Furthermore, an effective phase-locked loop (PLL) design is indicated by the Figure of Merit (FOM), which is -161.35 dB/Hz.

Discussion

The performance of the proposed PLL is compared with previously reported PLL architectures operating at lower frequency ranges. Although the design reported exhibits slightly lower phase noise, it operates within a much lower frequency range of 2–2.9 GHz (26). This operating figure-of-merit (FoM) of −161.35 dBc/Hz also indicates competitive performance when compared with other PLL implementations (27, 28). For instance, the architecture described uses 65-nm technology to achieve operation up to 7 GHz, whereas the designs reported operate below 2 GHz (28). Comparable to the low-noise performance reported, the proposed PLL achieves a phase noise of −104.05 dBc/Hz at a 1 MHz offset (27-29). Similarly, the design described operates at a single

frequency of 2.94 GHz while achieving −117.44 dBc/Hz phase noise (30). These comparisons indicate that the proposed architecture maintains comparable spectral purity while extending the operating range to the X-band region (8–12 GHz). Compared with earlier PLL implementations using older technology nodes such as 130-nm and 180-nm CMOS, the proposed 45 nm design demonstrates improved integration capability and stable high-frequency operation. For X-band operation, the achieved phase noise of −104.05 dBc/Hz at a 1 MHz offset demonstrates good spectral purity suitable for radar and high-frequency wireless communication systems. Another significant factor affecting PLL performance is the technology node exploited during implementation. 180-nm CMOS technology is used in the implementation of some earlier designs (30, 31), which frequently result in increased parasitic capacitances and restrict the attainable oscillation frequency. The proposed PLL offers increased integration density, reduced parasitic effects and faster transistor switching speed by utilizing a 45 nm CMOS technology. For modern RF integrated circuits operating in microwave frequency bands, these benefits allow for dependable high-frequency oscillation and enhanced scalability. For integrated PLL systems, power consumption is still a vital design factor. The comparison shows that previously disclosed systems have power consumption ranging from 0.18 mW to 18 mW, based on the architecture and technology node (26-31). The recommended PLL 9.6 mW power consumption makes sense given the significantly wider operational frequency range attained. Consequently, the design strikes a practical balance between power consumption and high-frequency operation that is appropriate for RF communication systems. Overall, the proposed PLL architecture provides a stable tuning range compatible with X-band frequency synthesis while maintaining competitive performance in terms of phase noise, power efficiency and tuning stability when compared with recently reported CMOS PLL designs.

Conclusion

This work employs 45 nm CMOS technology with a varactor-based VCO to successfully develop and implement a low-phase-noise X-band PLL (8–12 GHz). The suggested design is ideal for high-frequency applications like radar systems and wireless communication because it achieves improved frequency stability and minimal phase noise. The PLL's efficiency in noise performance is demonstrated by its measured phase noise of −104.05 dBc/Hz at 1 MHz offset, while operating at a reference frequency of 125 MHz. The design's better power efficiency (9.6 mW) and Figure of Merit (FoM) of -161.35 dBc/Hz are highlighted in a comparison analysis with previous studies, confirming its effectiveness in terms of energy efficiency and noise reduction. The findings verify that the suggested PLL offers the best possible balance between phase noise, frequency range and power consumption, making it a high-performance, small and affordable option for next-generation radar and radio frequency applications. Comparative results indicate that the proposed 45 nm PLL generates a broad X-band with low phase noise and lower power consumption while providing an effective trade-off between bandwidth, stability, lock time and noise performance. It is essential for small, battery-powered high-frequency transceivers in radar, satellite and upcoming 5G/6G systems due to its low power consumption. To further enhance phase noise, jitter performance and tuning flexibility, future research may concentrate on adaptive bandwidth control, fractional-N techniques and experimental validation of the proposed PLL architecture. Overall, the proposed PLL provides a small, energy-efficient and high-performance frequency synthesis solution with significant potential for next-generation radar and high-speed wireless communication systems.

Abbreviations

CMOS: Complementary Metal–Oxide Semiconductor, FMCW: Frequency-Modulated Continuous Wave, mmWave: Millimeter Wave, PNOISE: Periodic Noise Analysis, PSS: Periodic Steady-State Analysis, PVT: Process, Voltage and Temperature, RF: Radio Frequency.

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Author Contributions

Priya PA: conceptualization, methodology, analysis, original manuscript draft, Shiyamala S: supervision, validation of results, manuscript review, final editing.

Conflict of Interest

The author declares no conflict during the study.

Data Availability

No datasets were generated or analyzed during the current study.

Declaration of Artificial Intelligence (AI) Assistance

This manuscript was written by the authors without the use of generative AI or AI-assisted technologies. All content is original and has been created by the authors themselves.

Ethics Approval

Not Applicable.

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