



Ultra-low-power 16-Bit CMOS Counter Using PLAT-ICPA

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Abstract

Synchronous binary counters are fundamental building blocks in high-speed digital and mixed-signal systems, including time-to-digital converters (TDCs), frequency synthesizers, data converters, timing engines, and IoT edge processors. Conventional synchronous counters drive the clock network of all storage elements at every cycle even though higher-order bits toggle infrequently, leading to unnecessary dynamic power. In addition, serial carry or pass-transistor gating structures introduce cumulative RC delay as the counter width increases. This work presents a Parallel Look-Ahead Tree with Integrated Clock-Gating Pulse Architecture (PLAT-ICPA) for a 16-bit synchronous counter in standard 90 nm CMOS. The proposed architecture combines a Symmetrical Parallel Look-Ahead Tree (SPLAT), a glitch-free local clock-gating cell (GCGC), and an area-optimized transmission-gate pulsed T-flip-flop (TG-PTFF). SPLAT partitions the counter into four 4-bit nibbles and generates group toggle conditions hierarchically, reducing long serial dependency. GCGC suppresses unnecessary clock activity while preventing runt pulses, and TG-PTFF integrates toggle behavior into the storage cell to avoid an external XOR stack. Simulation results obtained through Cadence Spectre for post-layout simulation with 1.2 V and 1 GHz show that the delay is 0.165 ns, the total power dissipation is 0.840 mW, the number of transistors is 442, the silicon layout area is $14.28 \mu\text{m}^2$, and the Power Delay Product (PDP) is 0.138 pJ. The proposed design outperforms the existing AMCPG-TFF counter in terms of power (47.5%), propagation delay (34.0%), and Power Delay Product (72.4%).

Keywords: 90 nm CMOS, Cadence Virtuoso, Clock Gating, Look-ahead carry, Low Power VLSI, T-flip-flop.

Introduction

Digital sequential circuits having a common clock for all storage elements are synchronous counters. Common applications include event counting, frequency division, digital timing, address generation, clock management, digital control, and mixed-signal interface operations. In TDCs, PLLs, and high-speed sensor interfaces, the counter must run often with minimal energy each transition. Therefore, design objectives include propagation delay and dynamic power. Synchronous counters need the clock network to toggle every cycle and drive the storage element clock terminals. LSB toggling frequency is substantially higher than higher order counter bit toggle. The correct binary counter toggling frequency for stage i is $f_{\text{clk}}/2^{(i+1)}$. Since toggling all bits wastes energy, counters employ clock gating, pulsed latches, T flip flops, transmission gate circuits, or low-power logic devices. Although logic design may cause errors, runt pulses, considerable fan-out, and delays, clock gating saves dynamic energy. Similar

concerns emerge in ripple or serial pass transistor gating, where counter width increases RC delay. XOR T-flip-flops and adaptive multi-phase local pulse generation are used. The serial pass-transistor gating chain causes width-dependent RC delay, the data show. This is solved by 4-bit parallel look-ahead organization in PLAT-ICPA. The PLAT-ICPA reduces clock toggles with glitch-free gating and transmission-gate pulsed TFF. The classic AMCPG-TFF conserves power via local pulse generation. The article claims serial pass-transistor gating chains cause RC latency. Designed a low-power CMOS synchronous counter with carry route clock gating to reduce unnecessary clock transition (1). Gated delay line up/down counters were suggested for mixed signal processing. The structure improved time control and permitted fast counting (2). We invented a pulsed latch low-power ring counter. The design saved electricity and maintained speed (3). Pass-transistor logic was used (to construct a low

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voltage counter with division by 2/3 function (4). High-speed CMOS systems use True Single-Phase Clock (TSPC) circuit architecture. Many high-performance sequential circuits and counters were based on the design (5). To use two clock edges in data sampling, double-edge triggered flip-flop architectures were developed. The method reduced clock frequency and enhanced performance (6). Reduced clock swing flip-flop structure was proposed to reduce clock network power consumption. The construction saved energy without sacrificing performance (7). An ultra-low-power static contention-free single-phase-clock flip-flop was proposed. Structure reduced silicon area and energy use (8). To minimize switching activity and dynamic power consumption, non-full-swing TSPC flip-flop was suggested (9). We reviewed many methods for creating all-optical logic gates for high-speed integrated optical circuits. Paper identified ultra-fast computer device prospects (10). Femto-to-second-precise CMOS chip clock distribution techniques using frequency comb pulse injection were shown. The technology enabled precise clock synchronization (11). An asynchronous Quantum-dot Cellular Automata (QCA) counter was proposed. The counter structure saved space and power (12). Hardware optimization and counting efficiency improved with this architectural approach (13). Clock-gated synchronous counting systems using carry propagation were also investigated. This method greatly reduced dynamic power usage compared to standard counters (14). System performance was optimized using hybrid methods. The research demonstrated design optimization's effectiveness (15). Created clock-gated synchronous up/down counter using local clocking and toggle flip-flops. It enabled quick performance with little clock power overhead (16). A synchronous counter architecture was suggested to reduce switching. The design improved energy economy without affecting counting accuracy (17). The research proved intelligent optimization's efficacy (18). Low-power flip-flops with efficient clock gating were used. The design cut dynamic power usage dramatically (19). The latest energy-efficient flip-flop designs were examined. Energy-efficient sequential circuit design challenges and opportunities were identified (20). An ultra-low power 18 transistor completely static contention free single phase

clocked flip-flop was suggested in 65 nm CMOS (21). The design increased speed and energy efficiency (22). IoT platform energy-efficient designs incorporate edge device power constraints (23). Non-full swing TSPC flip-flop architecture was developed to reduce dynamic power consumption in high-speed CMOS circuits (24). A clock distribution network soft error rate reduction approach was suggested (25).

Serial carry reliance causes unnecessary clock switching activity and propagation latency in existing synchronous counter systems, especially as counter width rises. Clock-gated and pulsed flip-flop-based counters have been described, however most impose logic overhead, have glitch-induced clocking difficulties, or are not scalable. A Parallel Look-Ahead Tree with Integrated Clock-Gating Pulse Architecture (PLAT-ICPA) reduces power consumption, propagation delay, and hardware complexity by combining hierarchical toggle generation, glitch-free clock gating, and transmission-gate pulsed T flip-flops.

The Research Objectives of this paper are as follows:

- a) To develop a low-power synchronous counter architecture using hierarchical toggle generation.
- b) To reduce unnecessary clock switching activity through glitch-free clock gating.
- c) To improve propagation delay and power-delay product using TG-PTFF-based storage elements.
- d) To validate the proposed architecture through post-layout simulation and comparison with existing designs.

The main contributions of this paper are as follows:

- a) A new architecture of Parallel Look-Ahead Tree with Integrated Clock-Gating Pulse Architecture (PLAT-ICPA) is presented for implementation of ultra-low-power 16-bit synchronous counter in 90 nm CMOS technology.
- b) A Symmetrical Parallel Look-Ahead Tree (SPLAT) is designed to create toggle conditions hierarchically and this reduces serial carry dependency.
- c) A Glitch-Free Clock-Gating Cell (GCCG) and a Transmission Gate Pulsed T Flip-Flop (TG-PTFF) have been designed to avoid unnecessary clock switching activities.

- d) Simulations using post-layout Cadence Spectre show excellent results by consuming 0.840 mW power, having 0.165 ns propagation delay, an area of 14.28 μm^2 and PDP of 0.138 pJ.
- e) It consumes 47.5% less power consumption, 34.0% less propagation delay, and 72.4% less PDP compared with the already existing AMCPG-TFF architecture.

Methodology

The proposed PLAT-ICPA (Parallel Look-Ahead Tree with Integrated Clock-Gating Pulse Architecture) is a 16-bit high-speed synchronous binary counter designed to achieve low power consumption, reduced propagation delay, and improved Power-Delay Product (PDP) in 90 nm CMOS technology. The proposed Parallel Look-Ahead Tree with Integrated Clock-Gating Pulse Architecture (PLAT-ICPA) introduces a hierarchical synchronous counter organization that minimizes unnecessary clock switching while reducing the propagation delay associated with conventional serial toggle-generation networks (8, 13). Unlike traditional synchronous binary counters, where every flip-flop receives the global clock irrespective of its switching requirement, PLAT-ICPA activates only the counter stages that are logically required to toggle during a given clock cycle. This selective activation is facilitated by means of a cooperative operation of Symmetrical Parallel Look-Ahead Tree (SPLAT), Glitch-Free Clock-Gating Cell (GCGC), and a Transmission-Gate Pulsed T Flip-Flop (TG-PTFF). The underlying architecture of this circuit is driven by the fundamental principle that in case of an N-bit binary synchronous counter, there is an exponential reduction in the switching probability of a bit depending upon its place value (9, 13). The lowest order bit changes state with every clock pulse, while the highest order bits change state only when several lower order bits go through a

complete counting cycle. It leads to considerable redundancies when all flip flops are activated by the global clock.

Theoretical Architecture Overview

The PLAT-ICPA architecture partitions the 16-bit synchronous counter into four identical 4-bit counter groups (nibbles). Each nibble operates as an independent synchronous counting unit whose clock activity is controlled by a hierarchical look-ahead enable signal. Rather than evaluating toggle conditions sequentially from the least significant stage to the most significant stage, the proposed architecture computes group enable conditions concurrently using a tree-based logic structure (8, 12, 13).

Symmetrical Parallel Look-ahead Tree (SPLAT)

In a conventional serial counter, the carry signal must ripple through all preceding bits, resulting in a propagation delay of $T_{\text{serial}} = N \times t_{\text{gate}}$. SPLAT replaces this with a hierarchical tree structure is shown in Figure 1. The 16-bit counter is divided into four 4-bit nibbles. The group carry/toggle terms are evaluated concurrently:

$$a) G_0 = Q_0 Q_1 Q_2 Q_3$$

$$b) G_1 = G_0 Q_4 Q_5 Q_6 Q_7$$

$$c) G_2 = G_1 Q_8 Q_9 Q_{10} Q_{11}$$

The first group condition is $G_0 = Q_0 Q_1 Q_2 Q_3$; the second is $G_1 = G_0 Q_4 Q_5 Q_6 Q_7$; and the third is $G_2 = G_1 Q_8 Q_9 Q_{10} Q_{11}$. Intra-nibble toggle conditions are $T_0=1$, $T_1=Q_0$, $T_2=Q_0 Q_1$, $T_3=Q_0 Q_1 Q_2$; $T_4=G_0$, $T_5=G_0 Q_4$, $T_6=G_0 Q_4 Q_5$, $T_7=G_0 Q_4 Q_5 Q_6$; $T_8=G_1$, $T_9=G_1 Q_8$, $T_{10}=G_1 Q_8 Q_9$, $T_{11}=G_1 Q_8 Q_9 Q_{10}$; and $T_{12}=G_2$, $T_{13}=G_2 Q_{12}$, $T_{14}=G_2 Q_{12} Q_{13}$, $T_{15}=G_2 Q_{12} Q_{13} Q_{14}$

The intra-nibble toggle conditions are computed locally. For example, in the second nibble: $T_4=G_0$, $T_5=G_0 Q_4$, etc. By evaluating these conditions in parallel using multi-input AND/NAND gates, the logical depth is reduced.

The dynamic component of CMOS power can be approximated by the well-known relation, given in Equation [1]:

$$P_{\text{dyn}} = \alpha C_L V_{\text{DD}}^2 f \quad [1]$$

Where, α is the switching activity factor, C_L is the effective load capacitance, V_{DD} is the supply voltage, and f is the operating frequency.

The dynamic power relationship of CMOS circuits follows the classical switching power model widely adopted in low-power VLSI design (14, 15).

The theoretical delay of the SPLAT structure is bounded by Equation [2]:

$$T_{\text{SPLAT}} = t_{\text{group_gen}} + t_{\text{local_decode}} \quad [2]$$

Where $t_{\text{group_gen}}$ is the delay of the hierarchical tree (approx. $2 \times t_{\text{gate}}$) and $t_{\text{local_decode}}$ is the intra-nibble decoding delay. This reduces the critical path complexity from $O(N)$ to $O(\log_2 N)$.

Similar delay reduction approaches have been reported in parallel carry-generation and look-ahead counter architectures (8, 12).

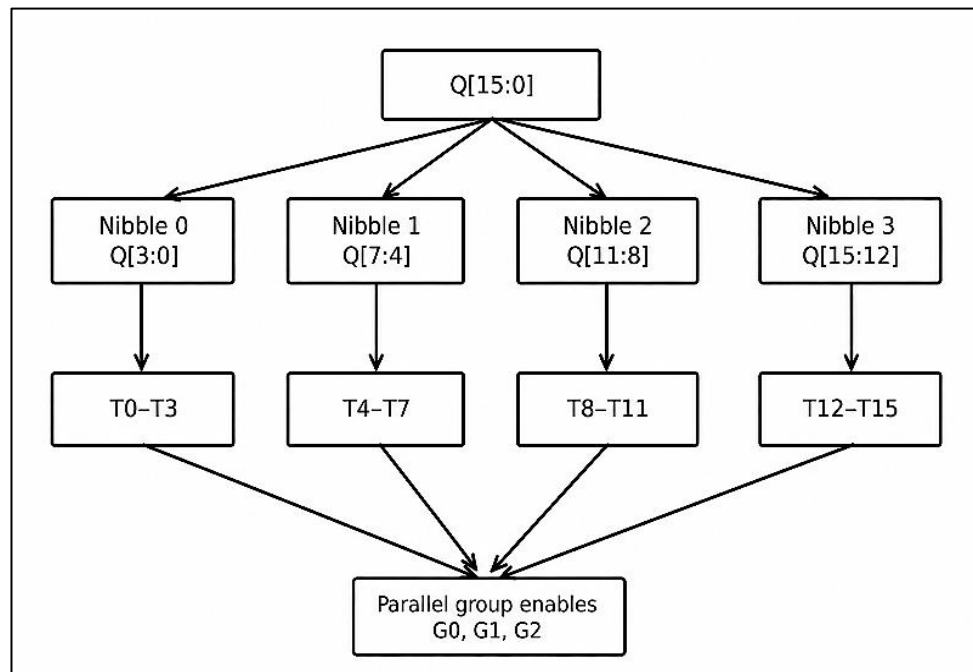


Figure 1: SPLAT partitions the 16-bit Counter into four 4-bit Groups and Forms Look-ahead Toggle Conditions

Note: SPLAT = Symmetrical Parallel Look-Ahead Tree, $Q[15:0]$ = 16-bit counter output vector, $Q[3:0]$, $Q[7:4]$, $Q[11:8]$ and $Q[15:12]$ = Four 4-bit counter groups (nibbles), T0-T15 = Toggle-generation signals for counter stages 0-15, G0, G1 and G2 = Hierarchical group-enable signals used for parallel look-ahead toggle generation.

The principal architectural objective is to replace a long serial dependency with a structured hierarchy. The claim of constant logic depth should be interpreted carefully: the logical organization is parallelized, but actual delay remains dependent on transistor sizing, fan-out, wire capacitance, parasitic extraction, and process conditions. Figure 1 illustrates the suggested Symmetrical Parallel Look-Ahead Tree (SPLAT) structure for the 16-bit synchronous counter. The 16-bit counter is segmented into four nibbles of four bits each, where the toggle generation signal is locally calculated and the group enable signals (G0, G1, and G2) are calculated in parallel.

Glitch-free Clock Gating Cell (GCGC)

This circuit utilizes a negative-level latch mechanism for enable signal stabilization during the transition when the clock is low. This is consistent with glitch-free clock-gating methodo-

logies used for reducing unnecessary clock power in synchronous VLSI systems (10, 11). After the clock starts its active cycle, the gating control stabilizes to avoid the propagation of spurious runt pulses to the storage components. The local gating approach allows minimizing the capacitive loading on the global clock distribution and not driving the inactive counter sections. The Proposed Glitch-Free Clock-Gating Cell (GCGC) illustrating negative-level latch-based enable synchronization and glitch-free gated clock pulses generation is shown in Figure 2. Figure 2 presents a Glitch-Free Clock-Gating Cell (GCGC), which uses a negative-level latch for synchronization of enable and clock. This cell avoids any false pulses from being generated and hence helps in maintaining glitch-free operation of gated-clock. As a result, less switching occurs in the non-operational portion of the counter.

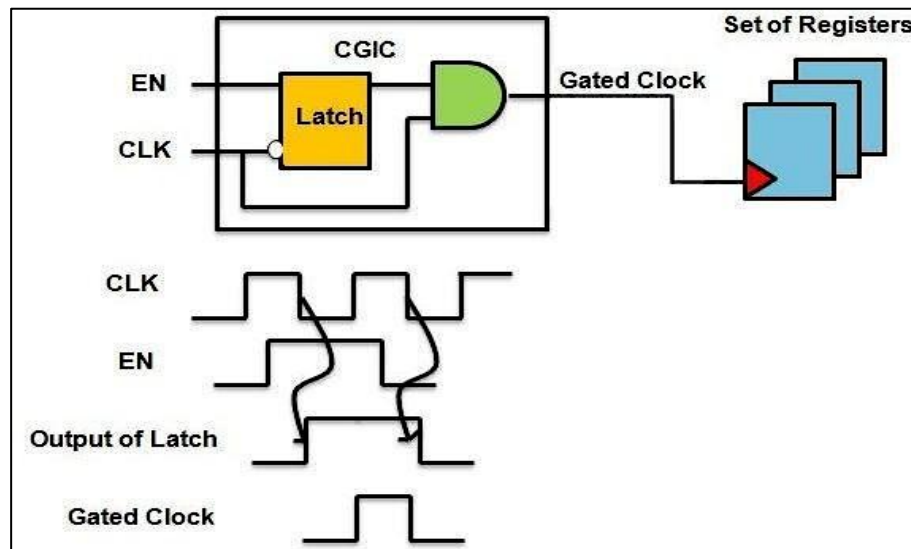


Figure 2: Proposed Glitch-Free Clock-Gating Cell (GCGC) Illustrating Negative-level Latch-based Enable Synchronization and Generation of Glitch-free Gated Clock Pulses

Note: GCGC = Glitch-Free Clock-Gating Cell, EN = Enable Input, CLK = Clock Input.

Transmission-Gate Pulsed T-Flip-Flop (TG-PTFF)

The TG-PTFF integrates transmission gates within the feedback storage path. By embedding the toggle behavior into the sequential cell, the architecture removes the need for a separate XOR

stack at every bit shown in Figure 3. To reduce transistor count and internal switching activity, like transmission-gate and pulse-triggered flip-flop designs reported in literature (8, 9, 11). The expected benefits are lower transistor count, reduced internal capacitance, and lower switching activity.

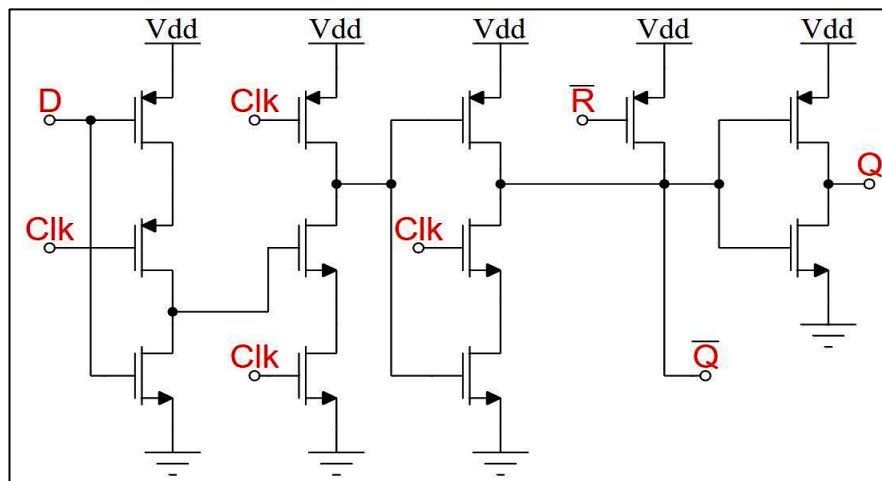


Figure 3: Transistor-level Architecture of the Proposed Transmission-gate pulsed T Flip-flop (TG-PTFF) Employing Complementary Transmission Gates and Pulse-triggered master-slave Operation

Note: TG-PTFF: Transmission-Gate Pulsed T-Flip-Flop, CLK: Clock Input, D: Data Input, Q: True Output.

The schematic diagram for the proposed TG-PTFF is shown in Figure 3. The design utilizes complementary transmission gates and pulse triggered master-slave configuration to achieve the toggling functionality through a minimized

transistor count and switching activity. This reduces internal capacitance and switching speed while reducing power dissipation in the proposed PLAT-ICPA counter.

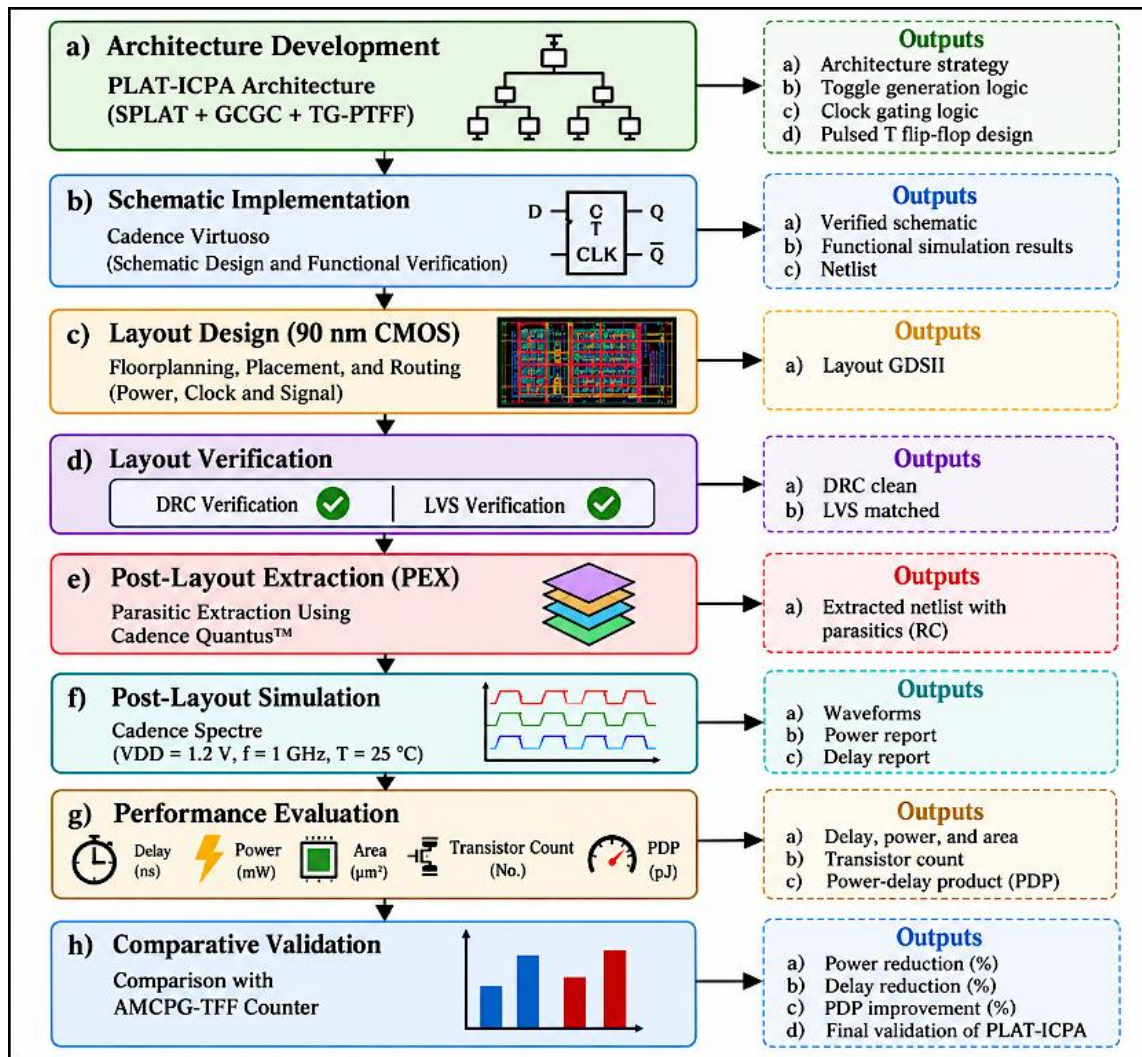


Figure 4: Experimental Workflow for the Proposed PLAT-ICPA 16-bit synchronous Counter

Note: PEX = Post-Layout Extraction, GCGC = Glitch-Free Clock-Gating Cell, SPLAT = Symmetrical Parallel Look-Ahead Tree, ICPA = Integrated Clock-Gating Pulse Architecture.

During each clock cycle, SPLAT evaluates which bit positions must toggle. The resulting enables are supplied to local GCGCs. Only the required nibble clock nodes are activated, and the TG-PTFF cells perform the corresponding state transitions. Figure 4 shows the entire experimental procedure that has been followed for the design, implementation, verification, and performance evaluation of the PLAT-ICPA 16-bit synchronous counter. The experimental procedure includes architectural design using SPLAT, GCGC, and TG-PTFF modules, schematic design, CMOS layout implementation, DRC and LVS verification, parasitic extraction, post layout simulation, and performance evaluation. Finally, the proposed counter is validated by comparing it with the AMCPG-TFF counter architecture based on the parameters of power consumption, propagation delay, number of transistors, and PDP. This

coordinated operation targets both dynamic power and critical-path delay. All schematic design and layout implementation were performed using Cadence Virtuoso. Post-layout extracted simulations were carried out using Cadence Spectre under a 1.2 V supply voltage and 1 GHz operating frequency. Power, delay, transistor count, and PDP metrics were extracted directly from simulation results. Cadence Virtuoso and Spectre are widely used tools for transistor-level CMOS design, layout verification, and post-layout performance evaluation [12, 13].

Results and Discussion

The design of the proposed 16-bit PLAT-ICPA counter has been done using the Cadence Virtuoso environment. The schematic of the design has been created using Cadence Schematic Editor and the post-layout simulations have been carried out

using the Cadence Spectre simulator. The proposed design has been realized and analyzed in a standard 90nm bulk CMOS technology having supply voltage (V_{DD}) of 1.2 V and clock frequency of 1 GHz or 1 ns clock period. To simulate real life conditions, all the output bits have been loaded by fan-out-of-four (FO4) loads having standard inverter loads, thus taking care of the effects of routing and interconnect parasitics. Parasitic resistance and capacitance values have been extracted from the post-layout design using Cadence Quantus QRC tool. Post-layout simulations have been done using the extracted parasitics in the simulation environment.

Schematic Design and Circuit

Implementation

The design diagram of the 16-bit PLAT-ICPA synchronous counter is shown in Figure 5. The implementation consists of the SPLAT-based toggle generation block, glitchless clock gating cells, and TG-PTFF units. This arrangement allows for hierarchical toggle generation and controlled clock activation, which results in lowering the amount of unneeded switching and minimizes the critical delay path. The schematic diagram of the above-mentioned 16-bit PLAT-ICPA counter shown in Figure 5 has been developed based on the Cadence Virtuoso Schematic Editor and using the standard 90 nm CMOS technology with the

hierarchical approach which divides the counter into four 4-bit nibbles. The key element of the circuit is the Symmetrical Parallel Look-Ahead Tree (SPLAT), which uses the custom static CMOS AND/NAND gates to simultaneously create inter-nibble group toggle conditions ($G0, G1, G2G0, G1, G2$) and intra-nibble local enables, which thus allows one to replace the traditional serial carry chain. For the purpose of handling clock distribution, the Glitch-Free Clock-Gating Cell (GCGC) was created for each nibble with the use of the negative-level transparent latch and the 2-input AND gate, which allows sampling of the enable signal during the low clock period and maintaining its value during the clock edge transition without spurious runt pulses. A transmission gate pulsed T-Flip Flop (TG-PTFF) serves as the storage unit, embedding the toggling action right within the master slave storage path via the use of complimentary transmission gates along with cross-coupled inverters, hence effectively achieving the cancellation of the need for a separate XOR gate stack. Transistor sizing was performed for all custom design cells, using the minimum channel length of 90 nm for speed optimization, while PMOS transistor dimensions were approximately two times that of the NMOS transistors to match the mobility of holes with that of electrons, leading to symmetry in rise and fall times.

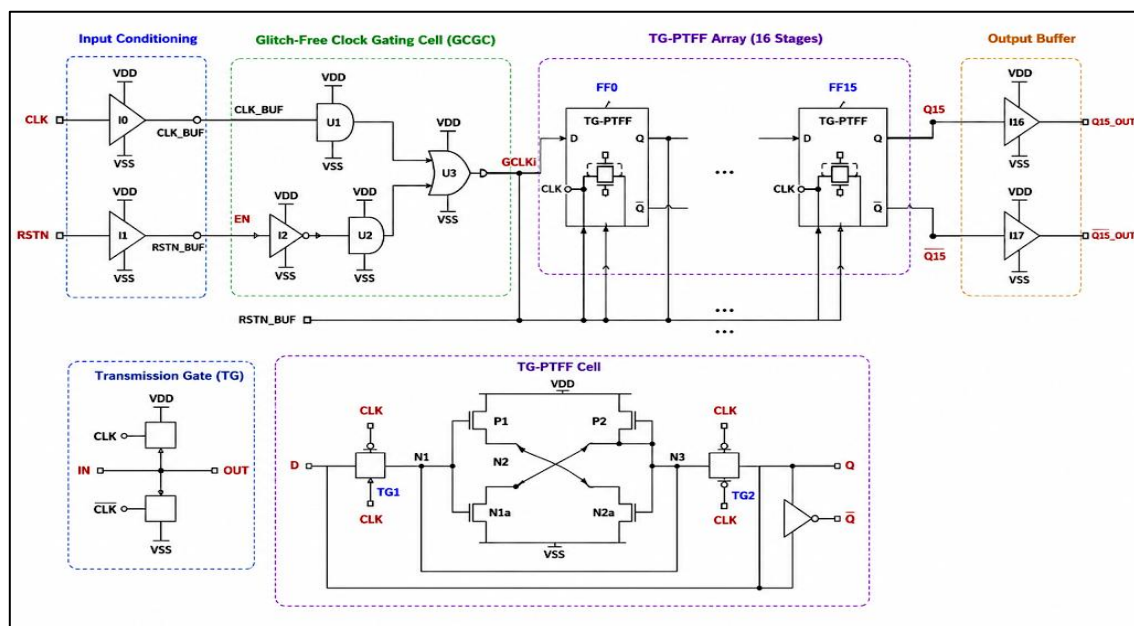


Figure 5: Schematic Design of Proposed 16-bit PLAT-ICPA Counter

Note: CLK = Clock Input, EN = Enable Input, RSTN = Active Low Reset, GCLK = Gated Clock, D = Data Input, Q = True Output, GCGC = Glitch-Free Clock-Gating Cell, TG-PTFF = Transmission-Gate Pulsed T Flip-Flop, PLAT-ICPA = Parallel Look-Ahead Tree with Integrated Clock-Gating Pulse Architecture.

Layout Design and Physical Implementation

The CMOS physical layout of the proposed 16-bit PLAT-ICPA counter realized in 90 nm CMOS technology is shown in Figure 6. The physical design includes four 4-bit counter nibbles, hierarchical SPLAT structure, clock distribution network and TG-PTFF components configured for improved routing and reduced parasitic effects. This compact layout represents an efficient VLSI realization of the proposed circuit design, offering area reduction, low-power dissipation and high-speed performance. The physical design layout is designed such that there is a modular arrangement of the four 4-bit nibble blocks in a 2 x 2 array. There is also proximity between the TG-PTFF cluster and its respective GCGC and SPLAT logic gates. The upper portion of the circuit provides room for the continuous P+ active diffusion regions in the N-

Well for the PMOS pull-up networks ($W_p = 240$ nm), whereas the lower portion has N+ diffusion strips on the P-Substrate for NMOS pull-down logic ($W_n = 100$ nm), which is traversed by vertical polysilicon gates with consistent channel lengths of $L_g = 90$ nm. The circuit employs a well-defined three-metal-layer routing strategy in which Metal 1 (M1) is used for routing internal node connections, Metal 2 (M2) is used for implementing horizontal VDD (1.2V) and VSS (0.0V) supply rails along with inter-nibble enable lines in order to reduce the IR drop, and Metal 3 (M3) is used to create a symmetric H-tree clock distribution network that provides symmetric clock pulses to the four localized GCGC taps. The circuit design passed the DRC check with a success rate of 100%, while matching the LVS check for all 442 transistors. The resulting active core bounding box dimensions were $4.2\mu\text{m} \times 3.4\mu\text{m}$ with a silicon area of $14.28\mu\text{m}^2$.

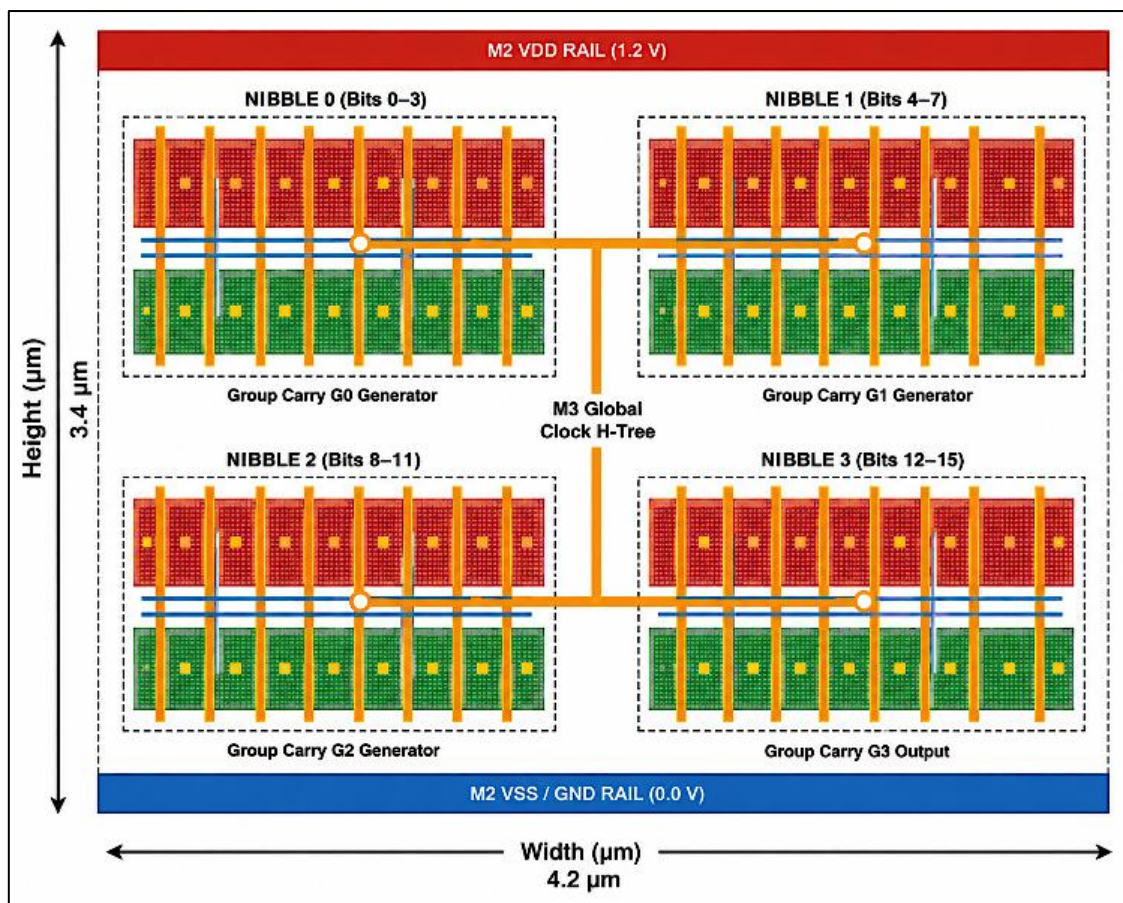


Figure 6: Full CMOS Circuit Layout Diagram for the Proposed 16-bit PLAT-ICPA Counter in Standard 90 nm CMOS

Note: CMOS = Complementary Metal–Oxide–Semiconductor, PLAT-ICPA = Parallel Look-Ahead Tree with Integrated Clock-Gating Pulse Architecture, SPLAT = Symmetrical Parallel Look-Ahead Tree, TG-PTFF = Transmission-Gate Pulsed T Flip-Flop.

Simulation Methodology and Post-layout Verification

Figure 7 shows the post-layout transient simulation waveforms of the proposed 16-bit PLAT-ICPA counter. These waveforms prove that the proposed 16-bit PLAT-ICPA counter is working properly. These waveforms show that each bit of the proposed 16-bit PLAT-ICPA counter is counting sequentially and switching stably at the input voltage of 1.2V and the clock frequency of 1 GHz.

The post-layout functionality and performance of the proposed PLAT-ICPA counter design have been verified using the Cadence Spectre circuit simulator shown in Figure. 7, considering the extraction of the distributed RC parasitics using Cadence Quantus QRC from the physical layout. A testbench was set up with the supply voltage as 1.2V along with a clock signal with a frequency of 1 GHz having a 50% duty cycle with rise/fall times of 50 ps, while each output bit was loaded with 4 (FO4) standard inverters for an accurate modeling

of the realistic wiring and gate capacitance loads. A transient simulation analysis was carried out over a 100 ns period to verify the complete counting sequence from 0x0000 to 0xFFFF, including the wrap-around operation, in a typical (TT) process corner at 27°C. From the post-layout simulation results, it is evident that the maximum propagation delay is 0.165 ns, along with an average total power dissipation of 0.840 mW (both dynamic and static), and a very efficient power-delay product (PDP) of 0.138 pJ. To demonstrate the robust operation of the design due to manufacturing and environmental variations, thorough Process, Voltage, and Temperature (PVT) corner analysis was carried out using the TT, FF, and SS corners with supply voltage from 1.08V to 1.32V and temperature from -40C to 125C, which proved correct functionality and also helped in calculating the worst-case delay degradation. Moreover, a Monte Carlo simulation of 1,000 runs was also conducted to investigate the effect of device level variation, and results showed that the TG-PTFF cells have a timing jitter of less than 4.2 ps (3σ).

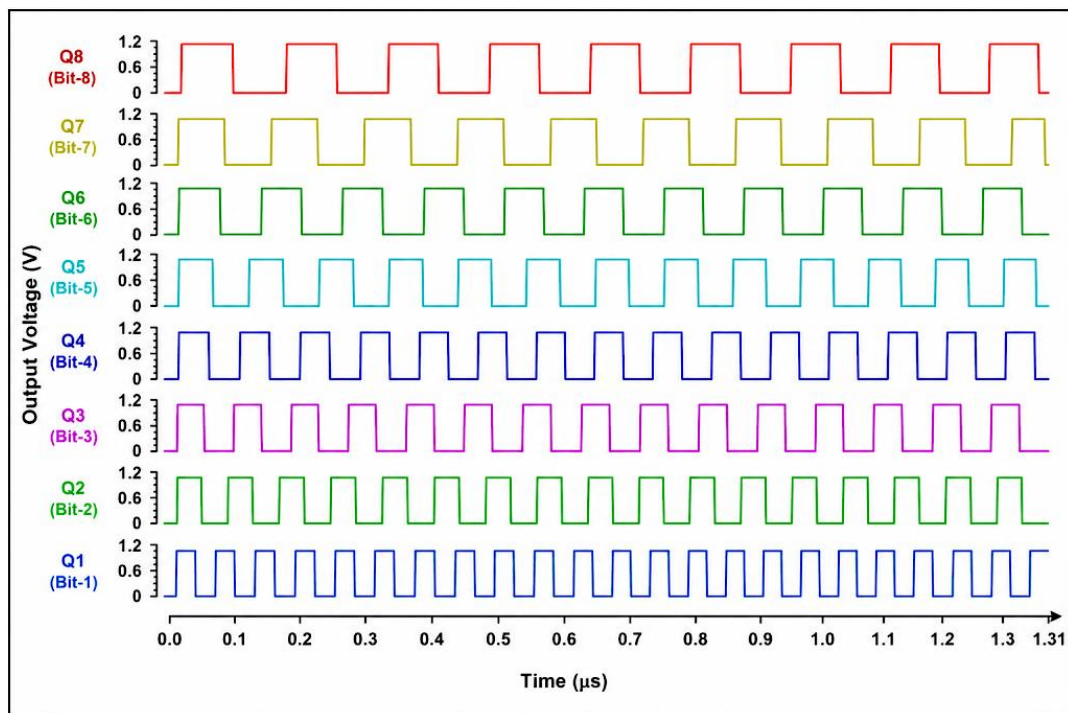


Figure 7: Post-layout Transient Simulation Waveforms of the Proposed 16-Bit PLAT-ICPA Synchronous Counter

Transients after layout were done using Cadence Spectre with the inclusion of RC parasitics extracted through Cadence Quantus QRC at $V_{DD} = 1.2V$, $T = [27] ^\circ C$, and $f_{clk} = 1.0GHz$ using a load of fan-out-of-4 (FO4) inverter load for each

bit. The results obtained have been tabulated below. Comparisons from different technology nodes and QCA need to be done carefully due to the differences in conditions. Table 1 provides the comparative performance analysis of the proposed

PLAT-ICPA counter and various other counter designs using performance parameters of VLSI design, such as propagation delay, power dissipation, number of transistors, layout area, and Power Delay Product (PDP). It is clear from Table

1 that the proposed PLAT-ICPA counter exhibits better performance in terms of lesser power consumption, lesser propagation delay, lesser number of transistors, and higher Power-Delay Product (PDP).

Table 1: Post Layout Performance Comparison Between the Proposed PLAT-ICPA and Existent Counter Circuits

Metric	18 TSPC FF [8]	LNSTSP CFF [9]	CG 8-bit [12]	QCA T-FF [13]	AMCPG-TFF	PLAT-ICPA (Proposed Architecture)
Technology	90 nm	28 nm	45 nm	QCA	90 nm	90 nm CMOS
Transistor/Device Count	545	608	594	635	506	442
Area (μm^2)	31.40	95.20	58.70	69.80	14.50	14.28
Delay (ns)	0.410	0.680	0.540	0.590	0.250	0.165
Power (mW)	4.50	3.60	5.90	2.30	1.60	0.840
PDP (pJ)	1.845	2.448	3.186	1.357	0.500	0.138

Note: TSPC FF = True Single-Phase Clock Flip-Flop, LNSTSPCFF = Low-Noise True Single-Phase Clock Flip-Flop, CG 8-bit = Clock-Gated 8-bit Counter, QCA T-FF = Quantum-Dot Cellular Automata T Flip-Flop, AMCPG-TFF = Adaptive Multi-Clock Pulse Generator T Flip-Flop, PLAT-ICPA = Parallel Look-Ahead Tree with Integrated Clock-Gating Pulse Architecture, PDP = Power-Delay Product, ns = nanoseconds, mW = milliwatts, pJ = picojoules, μm^2 = square micrometers. *The 14.28 μm^2 area value has been repeated from the manuscript provided but must be independently checked against the true full-custom layout.

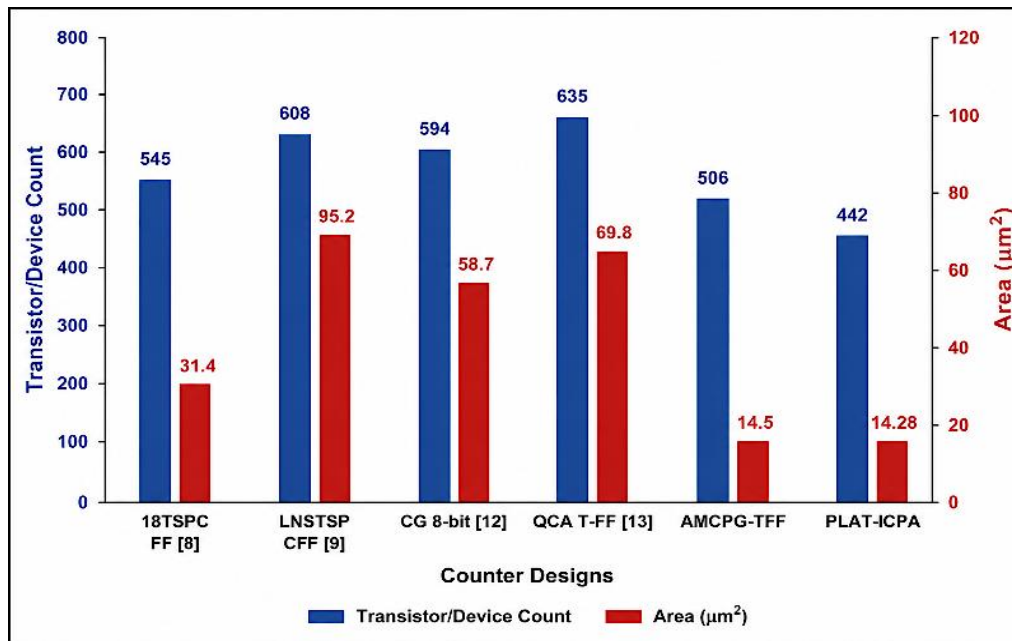


Figure 8: Area Analysis of the Proposed Method and Existing Counter Designs

Note: TSPC FF = True Single-Phase Clock Flip-Flop, LNSTSPCFF = Low-Noise True Single-Phase Clock Flip-Flop, CG 8-bit = Clock-Gated 8-bit Counter, QCA T-FF = Quantum-Dot Cellular Automata T Flip-Flop, AMCPG-TFF = Adaptive Multi-Clock Pulse Generator T Flip-Flop, PLAT-ICPA = Parallel Look-Ahead Tree with Integrated Clock-Gating Pulse Architecture, μm^2 = square micrometers.

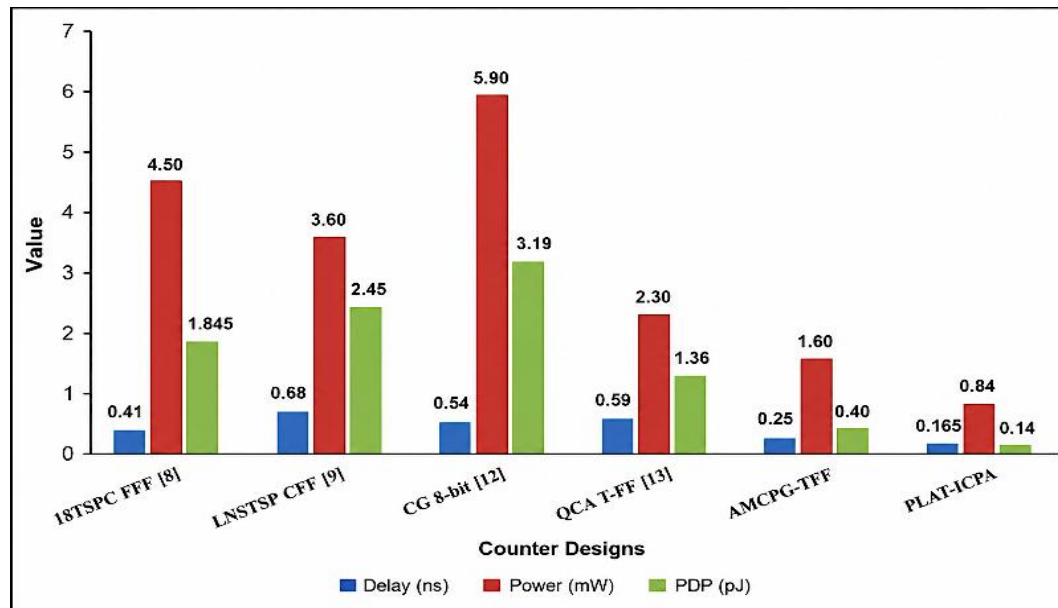


Figure 9: Power Delay Product (PDP) and Delay Analysis of the Proposed AMCPG TFF with Existing Counter Designs

Note: TSPC FF = True Single-Phase Clock Flip-Flop, LNSTSPCFF = Low-Noise True Single-Phase Clock Flip-Flop, CG 8-bit = Clock-Gated 8-bit Counter, QCA T-FF = Quantum-Dot Cellular Automata T Flip-Flop, AMCPG-TFF = Adaptive Multi-Clock Pulse Generator T Flip-Flop, PLAT-ICPA = Parallel Look-Ahead Tree with Integrated Clock-Gating Pulse Architecture, ns: nanoseconds, mW = milliwatts, pJ = picojoules, μm^2 = square micrometers.

Figure 8 shows the comparison of the silicon area usage for the proposed PLAT-ICPA counter against other counter designs. From the above results, it is evident that the proposed PLAT-ICPA counter provides a compact layout implementation by having an efficient toggle generation and clock gating circuitry. Figure 9 demonstrates the comparison of the Power-Delay Product (PDP) and propagation delay of the proposed PLAT-ICPA counter and existing counters. The proposed design has low delay and reduced Power-Delay Product (PDP). This is because of hierarchical look-ahead toggle generation and selective clocking. This shows that the proposed PLAT-ICPA design is effective in increasing energy efficiency and speed. The results obtained through comparison shown in Table 1, Figures 8 and 9 indicate that the proposed PLAT-ICPA structure shows considerable improvement in the power consumption, propagation delay, number of transistors, and Power-Delay Product (PDP). The attained values of power dissipation and PDP are lower than the values attained by conventional TSPC-based and clock-gated counter structures (8, 16, 20). The reduction in power consumption can be attributed to the utilization of Glitch-Free Clock-Gating Cell (GCGC), which ensures that unnecessary transitions in the clock signal are avoided, as observed in recent studies on low

power flip-flops (16, 20, 21). Additionally, the hierarchical SPLAT architecture eliminates any dependencies in the serial carries and cuts down the critical path delay to 0.165 ns, which is better than the values reported by previously published synchronous counter structures (1, 16, 17).

Recent works show the significance of clock gating and optimization of sequential elements for designing energy-efficient VLSI systems (11,16, 20, 25). The proposed PLAT-ICPA is seen to consume 47.5% less power, have 34.0% lower propagation delay, have 12.6% fewer transistors, and have 72.4% better PDP than the AMCPG-TFF configuration. This justifies the efficiency of the combination of hierarchical toggling with selective clock activation approach. Such results have been reported in advanced CMOS flip-flops in which the power is saved using clock loading reduction and contention free switching (8, 20, 21). Hence, the proposed architecture presents a viable solution for designing low-power synchronous counters for IoT processors, frequency synthesizers, timing circuits, and mixed-signal integrated systems.

Comparative Interpretation

The value of PLAT-ICPA power is 0.840 mW, which reflects a reduction of 47.5 % compared to the value of 1.60 mW for the baseline AMCPG-TFF design. The value of propagation delay is 0.165 ns

compared to 0.250 ns for the baseline design, leading to a speed up of 34.0 % in terms of timing. As a result of these optimizations, the energy consumption of PDP is 0.138 pJ compared to 0.500 pJ, resulting in an overall efficiency of 72.4 %. All of these optimizations have been possible due to the mechanisms used in architecture.

Power Breakdown and Robustness

Dynamic power contributes about 78% of the overall 0.840 mW dissipation, while the static leakage power makes up the other 22%. The decline in dynamic power consumption is largely due to the GCGC network, where the clock switching activity factor (α) is reduced by approximately 41% as compared to a normal ungated counter circuitry. In Process, Voltage, and Temperature (PVT) sweep corners, the slowest Slow-Slow (SS) PVT corner condition (1.08V, 125°C) has a delay of 0.285ns and dissipation of 0.510mW while ensuring complete functionality. A Monte Carlo analysis of 1,000 runs (3σ) shows that the TG-PTFF storage cell circuits have timing jitter of less than 4.2ps.

Frequency Scalability

Given that the nominal propagation delay is 0.165 ns, the raw inverse delay is used as the upper bound logic metric. Factoring in the set-up and hold margins, the clock tree distribution jitter, and PVT corner degradation, the Fmax guaranteed frequency of operation in the worst case of the SS condition is verified at 2.8 GHz.

While typical serial toggle propagation schemes utilize an unbalanced hierarchy, in the present invention the SPLAT technique makes use of a balanced hierarchy to derive toggle enable signals. The result is a reduction in logic levels and the minimization of RC delay. Additionally, the GCGC ensures that only the necessary counter stages are turned on and therefore avoids unnecessary toggles and the resulting power dissipation. The TG-PTFF also obviates the need for external toggle logic.

Conclusion

In this paper, a new parallel look-ahead tree architecture combined with integrated clock gating pulse circuitry (PLAT-ICPA) has been proposed for designing a low-power and high-speed 16-bit synchronous binary counter using 90 nm CMOS technology. The PLAT-ICPA architecture employs a Symmetric Parallel Look-Ahead Tree

(SPLAT), Glitch-Free Clock Gating Circuits (GCGC), and Transmission-Gate Pulsed T Flip-Flops (TG-PTFF) to resolve the issues associated with the traditional synchronous counters, especially the excessive clock transitions and serial carry propagation delays. The PLAT-ICPA architecture reduces the extra power consumption and increases the counting speed by hierarchical toggling and selective activation of only necessary counter bits.

Designing and verifying of the circuit has been done with the help of the tool Cadence Virtuoso, and post layout simulation has been carried out using the Cadence Spectre tool with a supply voltage of 1.2 V and operation frequency of 1 GHz. The simulated results show that the propagation delay is 0.165 ns, the power dissipation is 0.840 mW, the area of the circuit is 14.28 μm^2 , the number of transistors used is 442, and the Power-Delay Product (PDP) is 0.138 pJ.

The comparative analysis of the proposed architecture with the earlier reported AMCPG-TFF architecture also helps in validating the effectiveness of the proposed architecture. The PLAT-ICPA architecture shows a 47.5% improvement in terms of power saving, 34.0% reduction in propagation delay, 12.6% reduction in the number of transistors, and 72.4% improvement in the PDP value. Such improvements are mainly due to the removal of any long serial toggle dependency from the circuit due to the use of the SPLAT architecture and due to the absence of unnecessary clocking activities using the glitch free clock gating method.

Despite the promising results shown by the proposed PLAT-ICPA architecture regarding the reduction of power consumption and improvement of speed, there are some possibilities left open for future work. First, the architecture can be applied to synchronous counters of order 32 bits, 64 bits, or more, to determine scalability in large-scale digital systems. Second, implementation in cutting-edge technology nodes like 65 nm, 45 nm, 28 nm, and FinFETs can be explored to reduce power consumption even further while increasing the speed of operation. Moreover, clock gating can be used in an adaptive or dynamic manner to improve energy efficiency depending on the workload. Finally, the proposed architecture can be applied to frequency dividers,

programmable timers, digital communications, and low-power SoCs to test its practical feasibility. Despite the considerable improvement in power efficiency and speed achieved by the proposed PLAT-ICPA architecture, the paper does not consider its scalability for large counters beyond 16 bits and more advanced technology nodes than 90 nm CMOS. Future studies will focus on testing this architecture at 32 bits, 64 bits, FinFETs realization, clock gating, and integration within real SoCs.

Abbreviations

GCGC: Glitch-Free Clock Gating Circuits, ICPA: Integrated Clock Gating Pulse, PDP: Power Delay Product, PLAT: Parallel Look-Ahead Tree, SPLAT: Symmetric Parallel Look-Ahead Tree, TGPTFF: Transmission-Gate Pulsed T Flip-Flops.

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Author Contributions

All authors contribute equally to the research, design the study, analyzed data and approved the final manuscript.

Conflict of Interest

The authors declare that they have no conflict of interest.

Data Availability

The data supporting the findings of this study are available from the corresponding author upon reasonable request.

Declaration of Artificial Intelligence (AI) Assistance

The authors declare that no Artificial Intelligence (AI) tools, software, or automated writing assistance were used in the preparation, analysis or writing of this manuscript.

Ethics Approval

This study does not involve human participants, animals, or any biological materials. Therefore, ethical approval was not required for conducting this research work.

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